Runtime Mechanisms for Leakage Current Reduction in CMOS VLSI Circuits

Afshin Abdollahi
University of Southern California

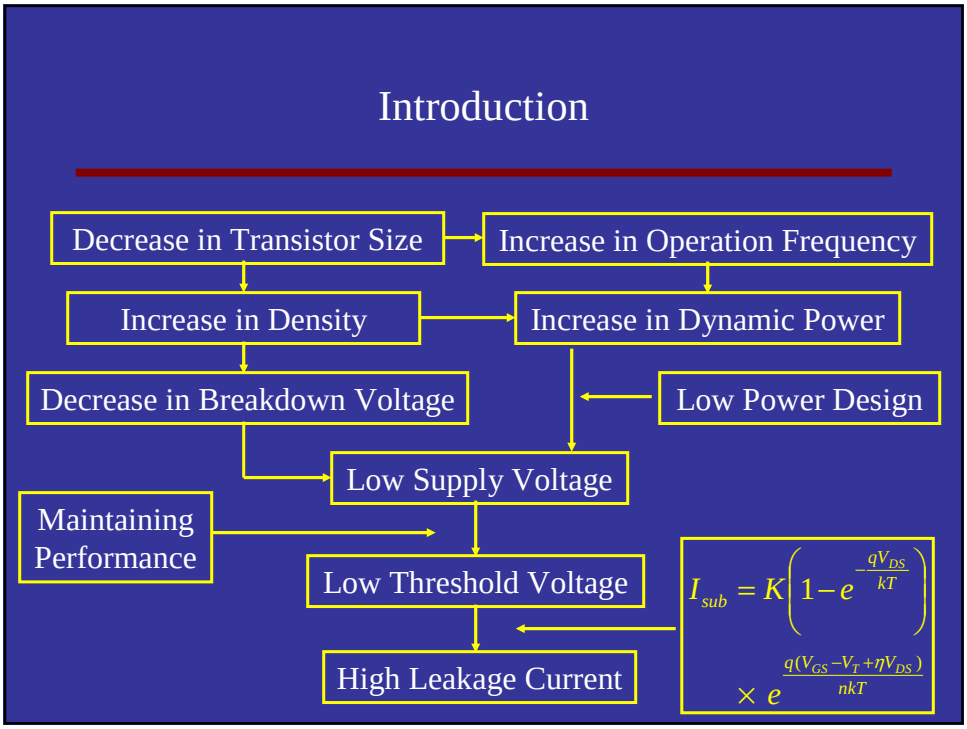
Farzan Fallah
Fujitsu Laboratories of America

Massoud Pedram
University of Southern California

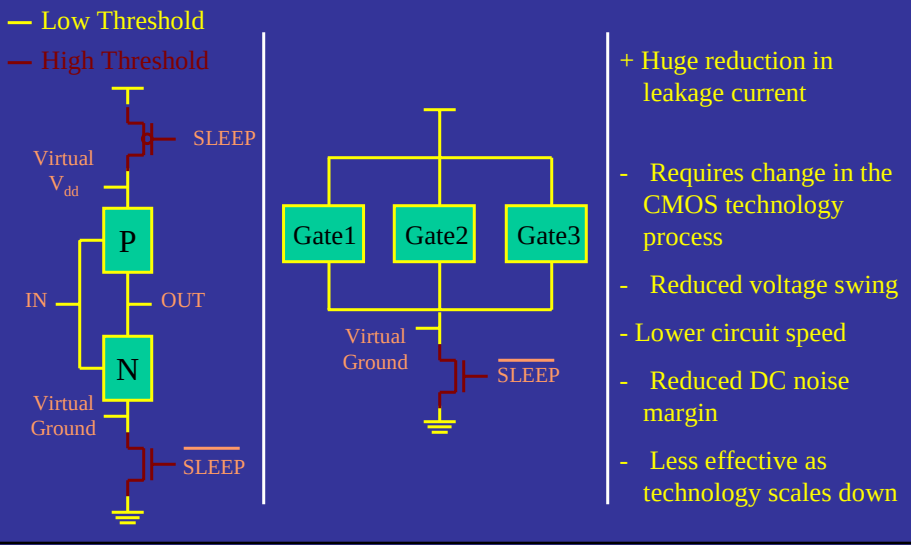
Outline

- Introduction
- Leakage Reduction Techniques
- Input Vector Control
- Adding Control Points
- Modifying Gates
- Results

Introduction



Power Supply Gating



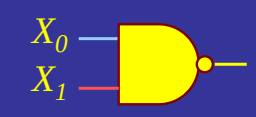
+ Huge reduction in leakage current

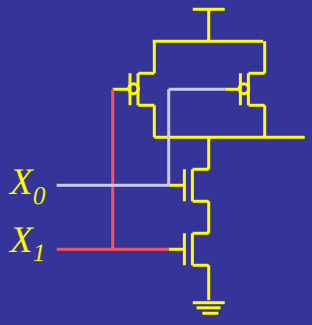
- Requires change in the CMOS technology process
- Reduced voltage swing
- Lower circuit speed
- Reduced DC noise margin
- Less effective as technology scales down

Dual and Variable Threshold Voltages

- Dual Threshold CMOS
  - . High-Threshold devices on non-critical paths
  - . Low-Threshold devices on critical paths
  - - Requires technology process modification
- Variable Threshold CMOS (VTCMOS)
  - . Dynamically change the substrate voltage to control the leakage and speed
  - . Substrate voltage higher than V_{dd} (for P transistors)
  - . Substrate voltage lower than Gnd (for N transistors)
  - - Requires triple-well technology and additional power supply
  - - Performance penalty (delay of retrieving the substrate voltage)
  - - Less effective as technology scales down

Input Dependence of the Leakage Current

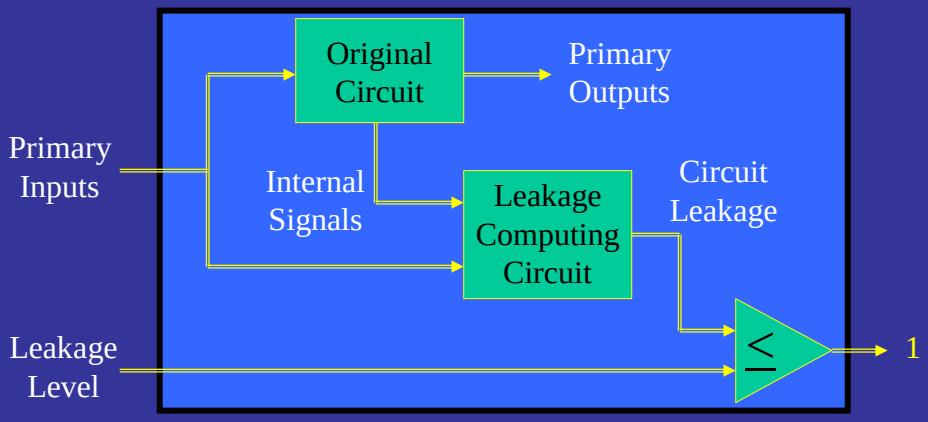




Technology: 0.18 micron
Supply Voltage = 1.5V
Threshold Voltage = 0.2V

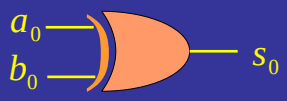
X_0 X_1	Leakage
0 0	23.60 nA
0 1	47.15 nA
1 0	51.42 nA
1 1	82.94 nA

Minimum Leakage Vector Identification



Search for the minimum leakage level for which the above Boolean network is satisfiable

Boolean Satisfiability Formulation



$s_0 = a_0 \oplus b_0$

a_0	b_0	s_0	clause
0	0	0	$cl_1 = a_0 + b_0 + \overline{s_0}$
0	1	1	$cl_2 = a_0 + \overline{b_0} + s_0$
1	0	1	$cl_3 = \overline{a_0} + b_0 + s_0$
1	1	0	$cl_4 = \overline{a_0} + \overline{b_0} + \overline{s_0}$

$\overline{a_0}\,\overline{b_0} \Rightarrow \overline{s_0}$

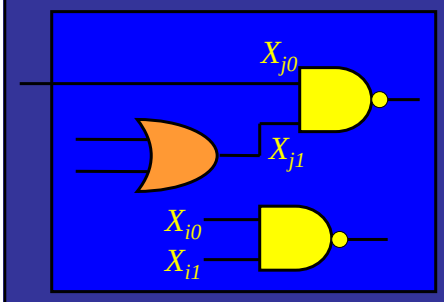
$\overline{\overline{a_0}\,\overline{b_0} + \overline{s_0}}$

$a_0 + b_0 + \overline{s_0}$

$l = AND(cl_1, cl_2, cl_3, cl_4)$

$(s_0 = a_0 \oplus b_0) \Leftrightarrow (l = true)$

Leakage Computing



0.18 micron

V_{DD} = 1.5V

V_T = 0.2V

X_j	Leakage	
0 0	23.60 nA	L_{00}
0 1	51.42 nA	L_{01}
1 0	47.15 nA	L_{10}
1 1	82.94 nA	L_{11}

-Quantize the leakage values to *k* levels:

$$D_{00}^j = \overline{X}_{j1}\overline{X}_{j0} \quad D_{01}^j = \overline{X}_{j1}X_{j0} \quad D_{10}^j = X_{j1}\overline{X}_{j0} \quad D_{11}^j = X_{j1}X_{j0}$$

$$Leakage\ (X_j) = D_{00}^j L_{00} + D_{01}^j L_{01} + D_{10}^j L_{10} + D_{11}^j L_{11}$$

Reducing Number of Additions

$$\left[\begin{array}{c}\text{Contribution of all NAND}\\ \text{gates to the total leakage}\end{array}\right] = L_{NAND} = \sum_{j=1}^{n} Leakage_{NAND}(X_j)$$

one bit *m bits*

$$L_{NAND} = \sum_{j=1}^{n}(D_{00}^j L_{00}) + \sum_{j=1}^{n}(D_{01}^j L_{01}) + \sum_{j=1}^{n}(D_{10}^j L_{10}) + \sum_{j=1}^{n}(D_{11}^j L_{11})$$

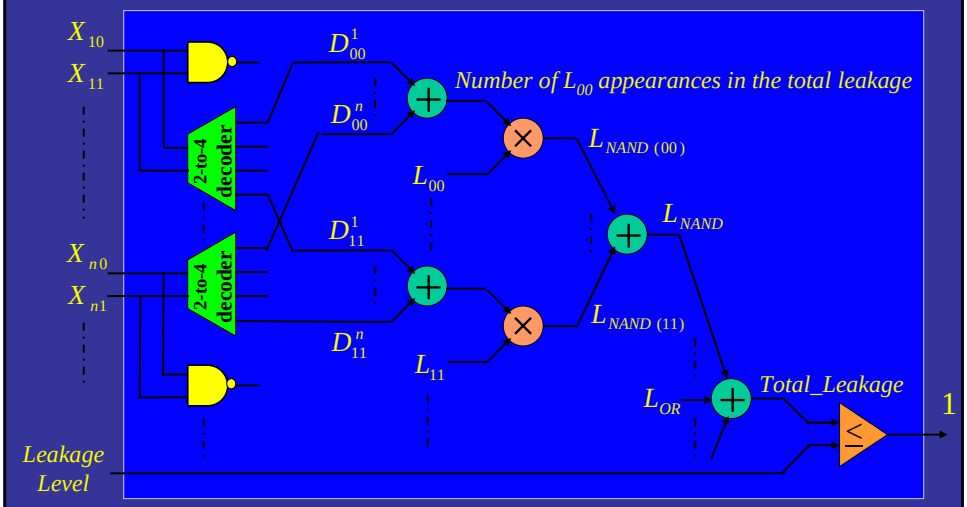
(n-1)m single-bit additions

log n bits *m bits*

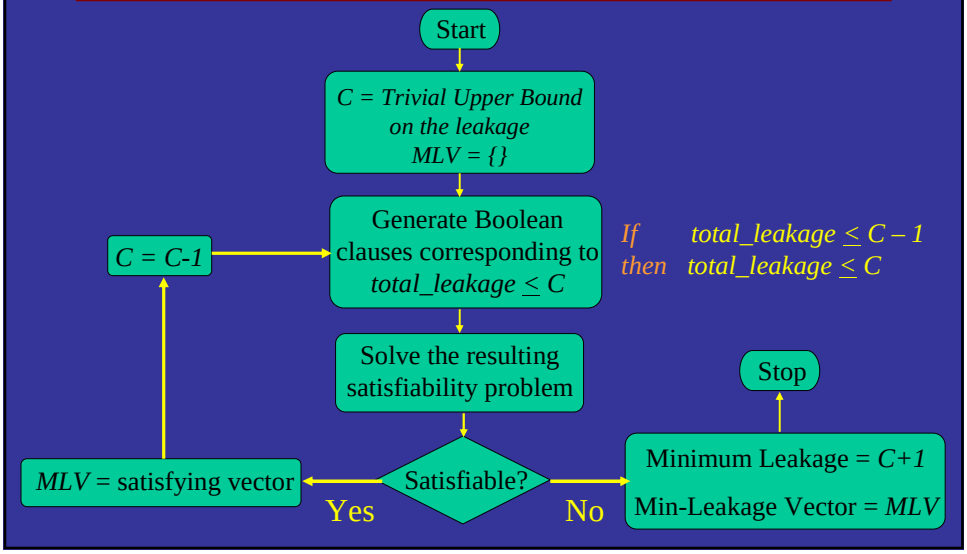
$$L_{NAND} = (\sum_{j=1}^{n} D_{00}^j)L_{00} + (\sum_{j=1}^{n} D_{00}^j)L_{00} + (\sum_{j=1}^{n} D_{00}^j)L_{00} + (\sum_{j=1}^{n} D_{11}^j)L_{11}$$

(n -1+ m log n) single-bit additions

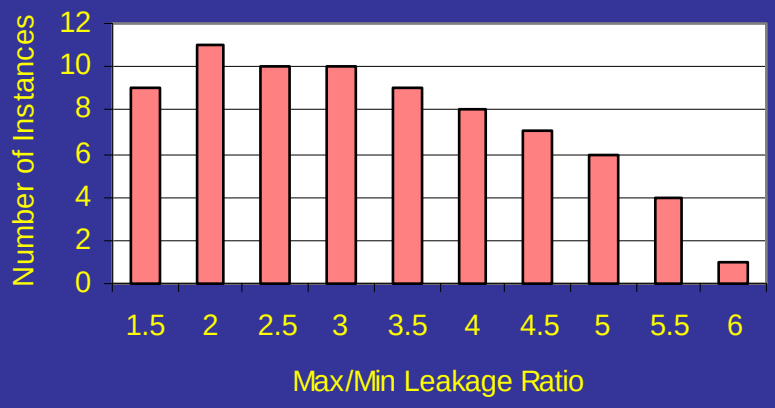
Leakage Computing Circuit



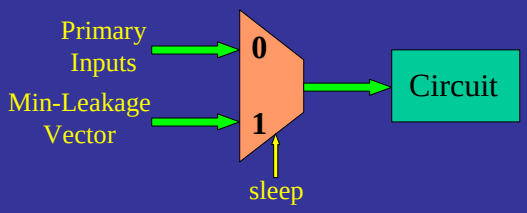
A Linear Search Algorithm for Minimum Leakage



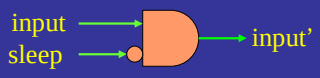
Comparing Maximum and Minimum Leakage Values



Applying the Minimum Leakage Vector

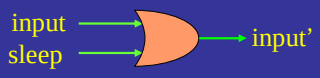


Min-Leakage Input = 0



sleep	input'
0	input
1	0

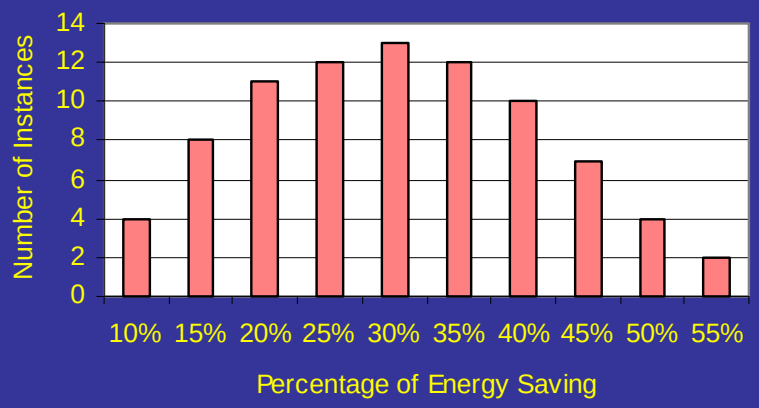
Min-Leakage Input = 1



sleep	input'
0	input
1	1

Input Vector Control

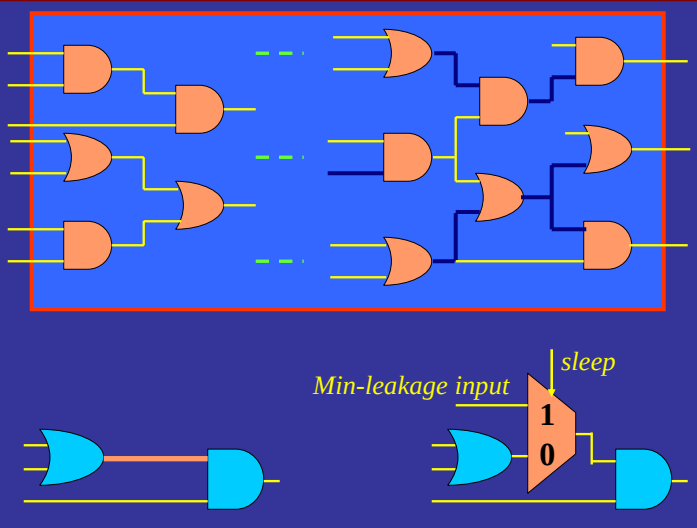
Leakage Power Reduction by Applying Min-Leakage Vector



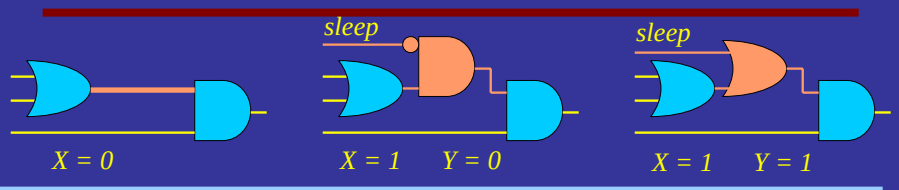
Comparing minimum leakage with average leakage in the standby mode

Adding Control Points

Controllability of Internal Gates



Adding Control Points



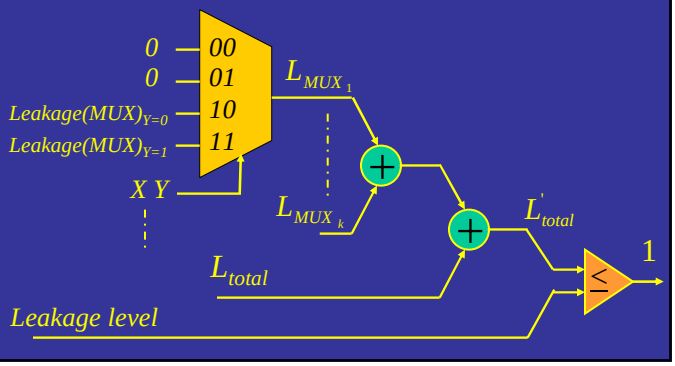
X Y Parameters

X = 0 : No change

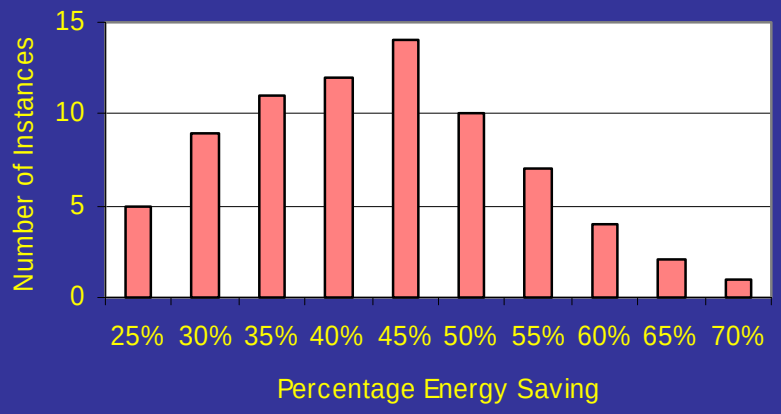
X = 1 : Multiplex with optimum value

Y = 0 : Optimum value = 0

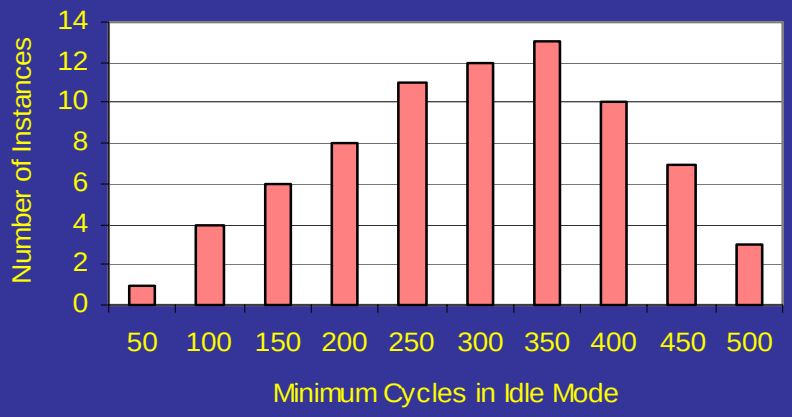
Y = 1 : Optimum value = 1



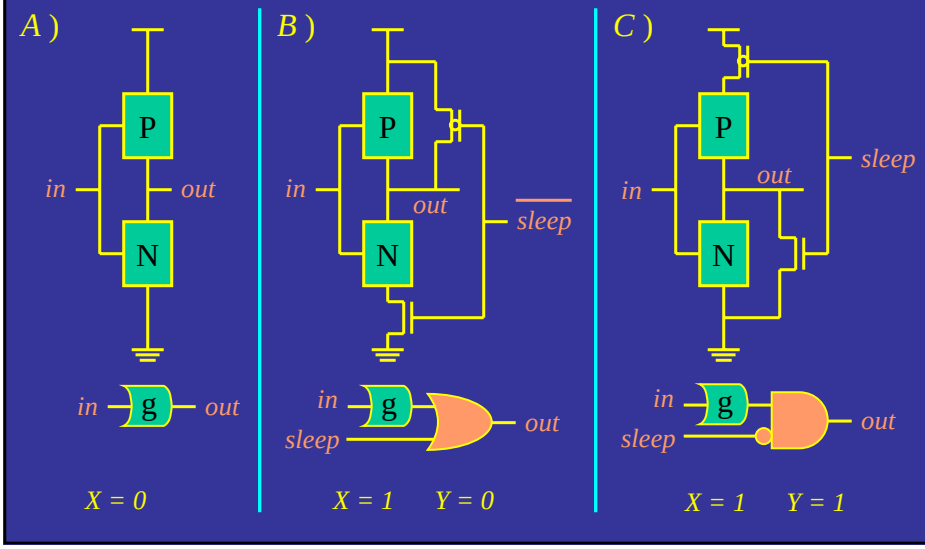
Power Reduction by Adding Control Points



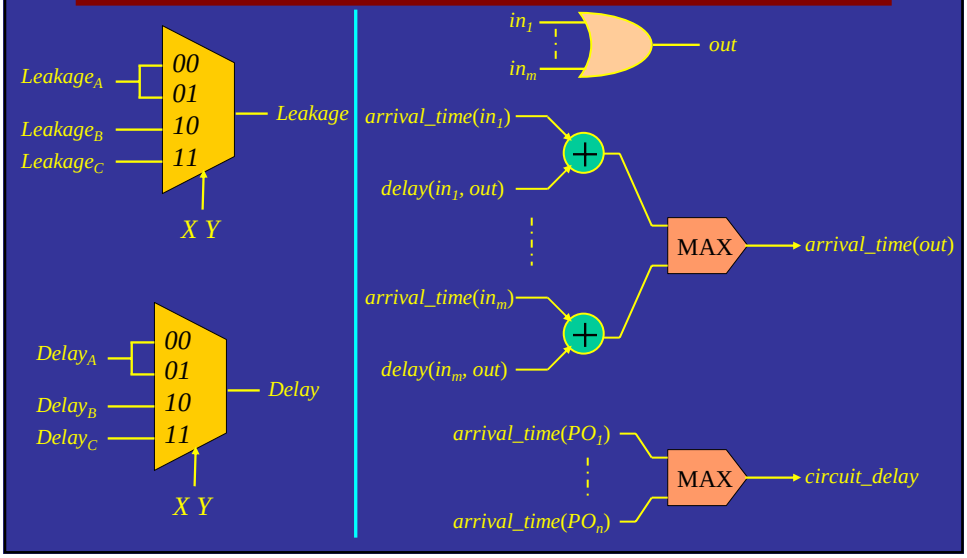
Breakeven Time



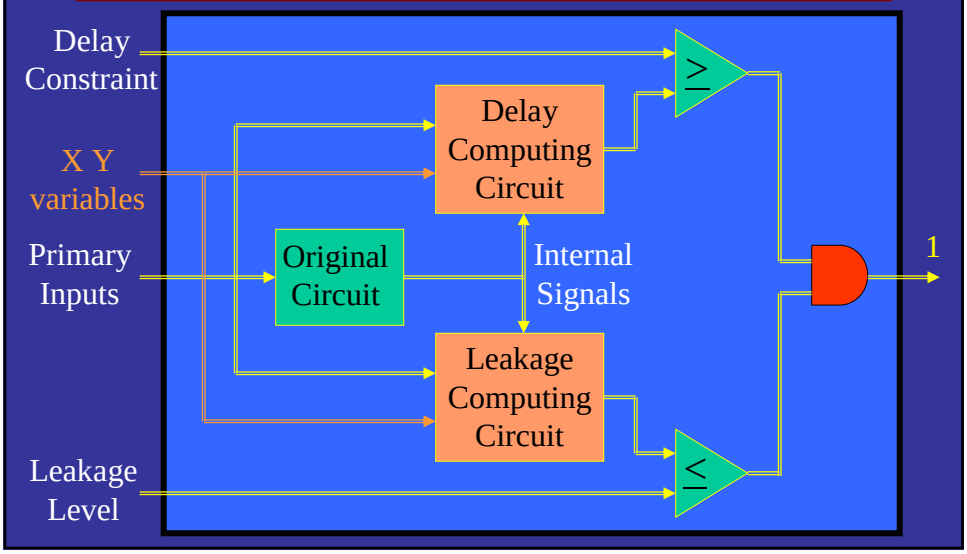
Modifying Gates



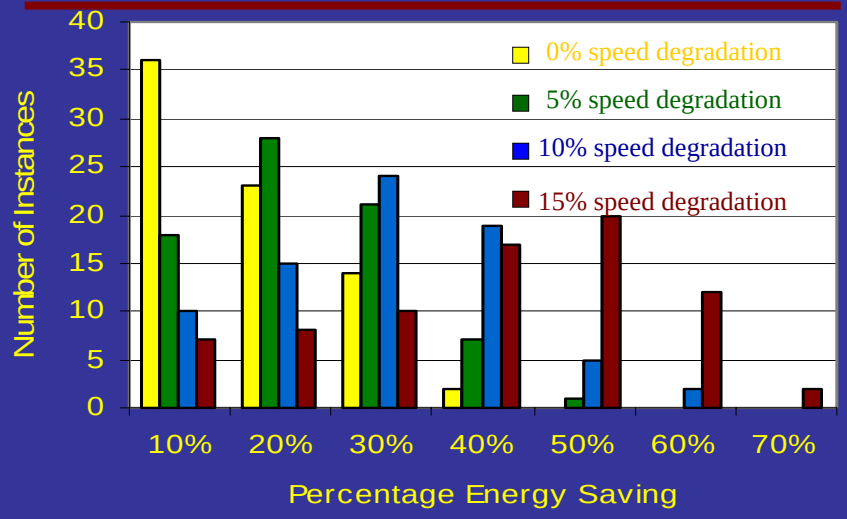
Delay Calculation



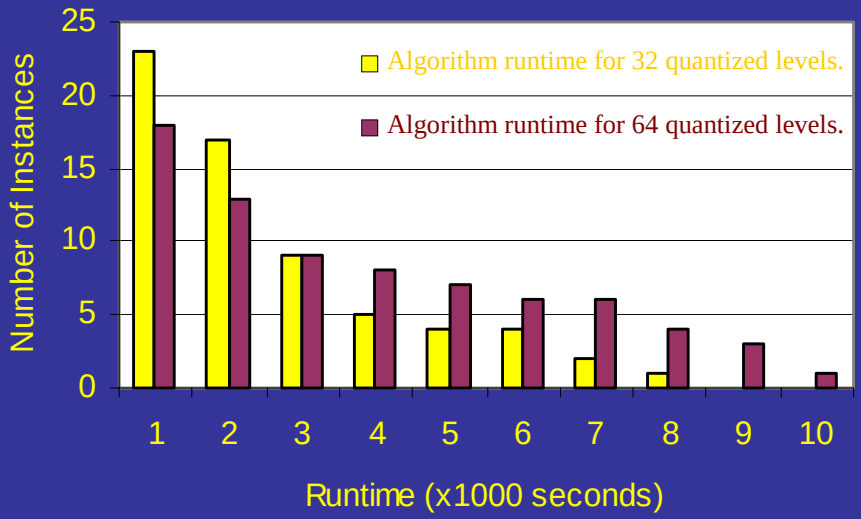
Equivalent Boolean Network



Energy Saving for Different Speed Degradations



Runtime of the Algorithm



Conclusions

- Two runtime mechanisms for reducing the leakage current of a CMOS circuit are presented
  - A "sleep" signal is used to shift in a new set of external inputs and pre-selected internal signals into the circuit so as to minimize the total leakage current in the circuit
  - NMOS and PMOS transistors are added to some of the gates in the circuit to increase the controllability of the internal signals of the circuit and decrease the leakage current of the gates using the "stack effect"
- Experimental results on the circuits in the MCNC91 benchmark suite demonstrate that it is possible to reduce the leakage current by up to 70% in VLSI circuits at the expense of a very small overhead.