Memory Bus Encoding for Low Power: A Tutorial

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Outline

- Background
- Memory Bus Encoding Techniques
  - Algebraic codes
  - Permutation codes
  - Probabilistic codes
- Conclusions

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Power Dissipation Equation

- $P \sim V^2 C f N$
- Low Power Techniques
  - Voltage Scaling
  - Capacitance Reduction
  - Frequency Scaling
  - Switching Activity Reduction
- Memory Modules
  - Fixed
  - High
  - High
  - Memory Bus Encoding

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Bus Encoding Example

- Binary Code

A1: 0000
A2: 0001
A3: 0010
A4: 0011
SA=6

- Gray Code

B1: 0000
B2: 0001
B3: 0011
B4: 0010
SA=4

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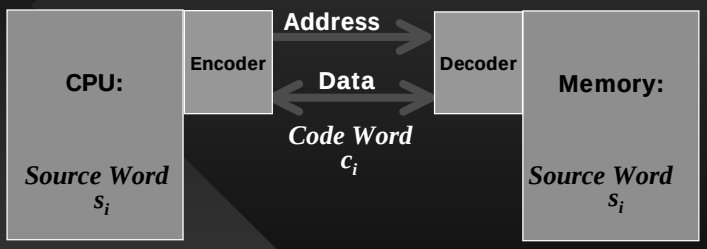
Generic Bus Encoding Architecture



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Bus Encoding Taxonomy

Redundancy	Irredundant:	Gray, Pyramid
	Redundant:	T0, Bus Invert, Working Zone
Circuit	Non-terminated	TTL, LVCMOS
	Terminated	RAMBUS, GTL
Signal Level	Level Signaling	
	Transition Signaling	
Location	On-chip Bus	Between CPU core and Caches
	Host Bus	Between Pentium and Chipset
	Memory Bus	Between Chipset and DRAM
Address/Data	Separated	
	Multiplexed	
Multiplexing	Non-multiplexed	SRAM
	Multiplexed	DRAM

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Code Classification

1. Algebraic Codes

   c_i *op x* : *op* is a binary operation

2. Permutation Codes

   $f(c_i)$: *f* is a fixed function

3. Probabilistic Codes

   $f_x(c_i)$: f_x is an application-specific function

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1 Algebraic Framework

- Decoding
  - c_i *op x*
- Notation

  <{x},op>

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Bus Invert: <*{0,1},XOR*>

- Stan, TVLSI 1995
- Extra signal: *INV*

  $s_i = c_i$, *if INV=0*

  $s_i = c_i$ *xor 1,* *if INV=1*
- Encoding
  - Hamming distance

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Partial Bus Invert: <*{0,x},XOR*>

- Shin et al., ISLPED 1998
  - Bus Partitioning
- Extensions
  - M-redundant Bus Invert
    - Spatial partitioning
  - Interleaving Partial Bus Invert, ICVC 1999
    - Temporal partitioning

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Transition Signaling: $<\{c_{i-1}\},XOR>$

- Decoding function

  $s_i = c_i \; XOR \; c_{i-1}$

- Efficient when c_i and c_{i-1} are similar

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T0: $<\{s_{i-1}\},Add,1>$

- Benini et al., Great Lakes VLSI Symp. 1997
- Extra signal: *INC*

  $s_i = s_{i-1}$ *add 1,* *if INC=1*

  $s_i = c_i$, *if INC=0*

- Effective for sequential access patterns
- Prediction

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Prediction-based: <{s_{i-1}},XOR,1>

- Ramprasad et al., TVLSI 1999
  - Inc-Xor
- Fornaciari et al., CODES 2000
  - Offset-Xor
  - T0-Xor
- For sequential access patterns

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Hybrid Encoding

- Benini et al, DATE 1998
- Instruction/Data interleaving
- T0 for instructions; Bus Invert for data
- Examples
  - T0_BI
  - Dual_T0
  - Dual_T0_BI

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Working Zone: *{a[],ADD}*

- Musoll et al, TVLSI 1998
- Instruction/Data segments
- Offset
- One-hot coding

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Comparison

• Binary	Ø	Identity
• Bus Invert	{0,1}	XOR
• Partial Bus Invert	{0,x}	XOR
• Transition Signaling	$\{c_{i-1}\}$	XOR
• T0	$\{c_{i-1}\}$	ADD_1
• Inc-Xor	$\{c_{i-1}\}$	XOR_1
• Working Zone	{x[]}	ADD

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2. Permutation Codes

- Fixed function: $f(c_i)$
- Irredundant
- Do not need the previous word s_{i-1} or c_{i-1}
- Examples
  - Gray code
  - Pyramid code
- For sequential access patterns

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Gray Code

- Su et al., ISLPED 1995
- Only one transition between consecutive words
- For address busses

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Pyramid Code

- Cheng et al., ISPLED 2000
- For multiplexed DRAM address busses
- No transition between consecutive words
- 50% switching activity reduction

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3. Probabilistic Code

- Given a program trace
- Statistics Information
  - First-order: $f(c_i)$
  - Second-order (pair-wise): $f(c_{i-1}, c_i)$
- Examples
  - Static analysis
    - Limited-weight code, Beach code, Clustered and Discretized code
  - Dynamic analysis
    - Adaptive, Codebook-based

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Limited Weight Code

- Stan et al., TVLSI 1997
- *K*-limited code
- First-order analysis
- First-order encoding

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Beach Code

- Benini et al., TVLSI 1998
- Second-order analysis
- First-order encoding

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Entropy-reduced Framework

- Ramprasad et al., TVLSI 1999
  - Functions
    - *F*: predict
      - Identity
      - increment
    - *f1*: error
      - Xor
      - Difference
    - *f2*: entropy
      - Invert
      - Probability (pbm)
      - Value (vbm)
  - Examples

Code-name	*F*	*f1*	*f2*
xor-pbm	identity	xor	pbm
inc-xor	increm	xor	identity

- Second-order analysis; First-order encoding
- $<\{s_{i-1}\}, xor \bullet f(c_i)>$

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Transition Encoding

- Benini et al, DAC 1999
- Second-order analysis
- Second-order encoding
  - Encode transitions instead of words
- Static
  - Exact
  - Clustered
  - Discretized
- Adaptive

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Codebook

- Komatsu et al., Great Lakes VLSI Symp. 1999
- Second-order analysis
- Second-order encoding
- Sort and encode dynamically

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More Recent Work

- Coupling-driven encoding
  - Kim et al., ICCAD 2000
  - Sotirsadis et al., ICCAD 2000

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Conclusions

- Encoding can reduce the switched capacitance on a bus
- Different types of codes have been proposed, each applicable to a particular type of bus and data access pattern
  - Algebraic codes
    - *<{x},op>*
  - Permutation codes
  - Probabilistic codes
    - Analysis/Encoding
      - First-order
      - Second-order
    - Static vs. Adaptive

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