Effects of Non-Uniform Substrate Temperature on the Clock Signal Integrity in High Performance Designs

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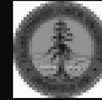

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Presentation Outline

- Introduction
- Analysis of Chip Temperature Profile
- A Non-Uniform Temperature-Dependent Performance Metric
- Effects on the Clock Skew
- Summary

Sources of Chip Power Dissipation

- Chip temperature increase is proportional to the increase in chip power dissipation
- Devices: Closer to the heat sink
  - Dynamic Power: $\propto CV^2f$ ⟶ most significant
  - Leakage Power: increases with scaling
- Interconnects: Farther from the heat sink
  - Joule Heating: $\propto I^2R$

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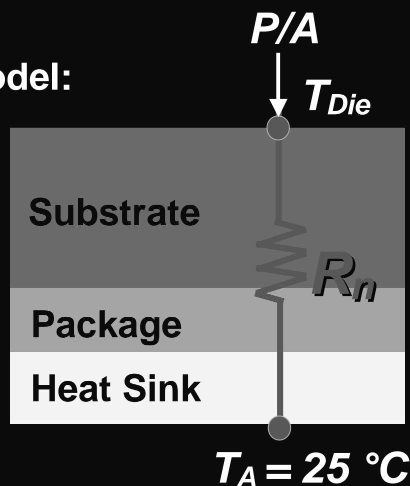
Average Chip Thermal Model

- 1-D heat conduction model:

$$T_{Die} = T_A + R_n \left(\frac{P}{A} \right)$$

- T_{Die} = 120 °C (180 nm)
- R_n = 4.75 cm² °C/W
- Assuming fixed packaging and cooling technologies, T_{Die} can be calculated for any technology node



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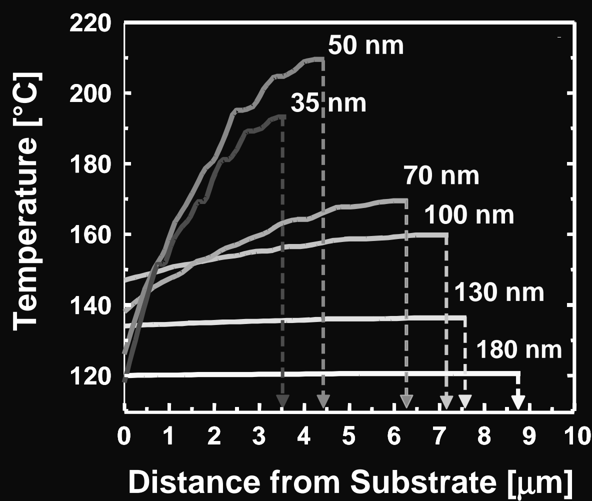
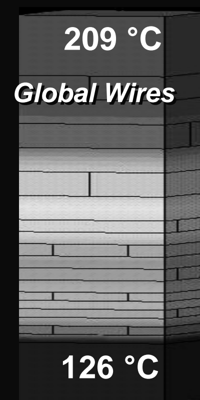
Thermal Effects in Interconnects

- Die power dissipation density remains approximately constant with the scaling down of feature size (*ITRS '99*)
- Interconnect Joule heating plays a very important role in the interconnect thermal profile
- By scaling, long global interconnects getting more closer to the substrate

Interconnect Temperature Distribution

- *Im and Banerjee* (*IEDM 2000*)





50 nm Node

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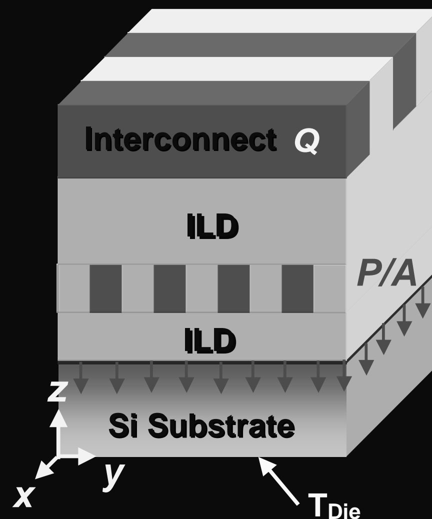
Full Chip Thermal Modeling

Three dimensional heat conduction in steady state

$$\nabla^2 T = 0$$

With an effective heat generation Q in the interconnect and a constant thermal conductivity k

$$\nabla^2 T + \frac{Q}{k} = 0$$



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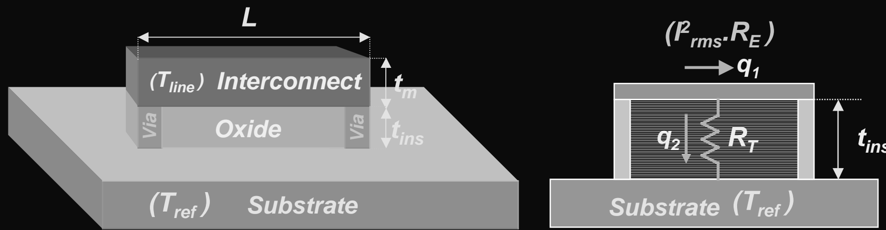
1-D Heat Equation for Interconnects



$$\frac{d^2T_{line}}{dx^2} = -\frac{Q}{k_m}$$

$Q = q_1 - q_2$

$$\frac{d^2T_{line}(x)}{dx^2} = \lambda^2 T_{line}(x) - \lambda^2 T_{ref}(x) - \theta$$

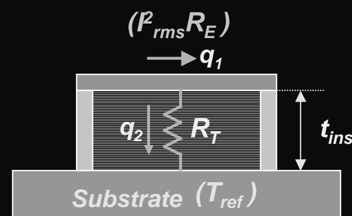
λ and θ are constants
$f(L, t_m, k_m, t_{ins}, k_{ins}, I_{rms}, R_E)$

Assumptions

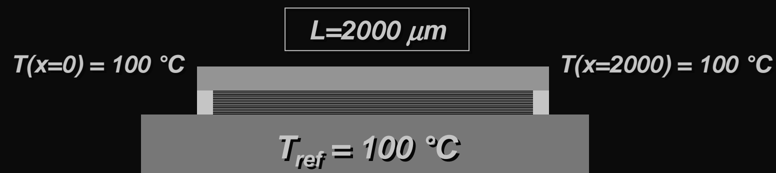
- Heat transfer in long interconnects takes place along the length of the line only
- Thermal conductivities k_m and k_{ins} remain constant
- Energy is only exchanged through the bottom side of the line
  - Four side walls and top side are adiabatic
  - Substrate acts as the heat-sink for the interconnect

Parameters Affecting $T_{line}(x)$

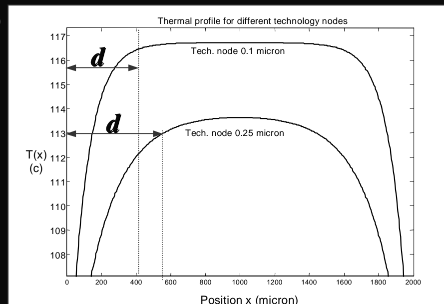
- RMS current
- Insulator thickness
- Wire width
- Insulator thermal conductivity
- Substrate temperature



Uniform Substrate Temperature

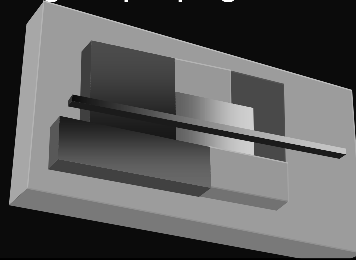


(NTRS'97)



Non-Uniform Substrate Temperature

- Substrate temperature is generally non-uniform
  - Functional block clock gating or dynamic power management can result in significant switching activity variations across a chip
  - Thermal propagation time constant is much larger than the signal propagation time constant



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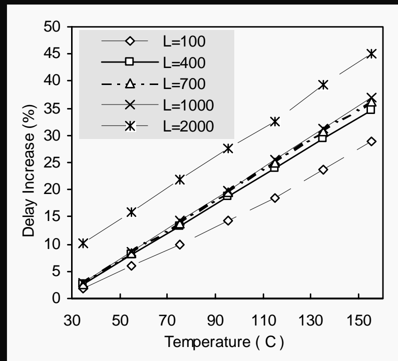
Temperature Dependency of Resistance

- Electrical resistance is dependent on temperature $r(x) = \rho_0(1 + \beta T(x))$



- ρ_0 : resistance per unit length at reference temperature
- β : temperature coefficient of resistance (1/°C)
- 5-6% delay increase for each 20-degree ***uniform*** temperature increase

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Non-Uniform Interconnect Thermal Profile

- Long global interconnects span a large area
  - High probability of experiencing the substrate thermal non-uniformities
- Assuming a uniform substrate thermal profile can result in overestimating performance degradation due to temperature
  - Introduces error in wire-planning for different optimization steps

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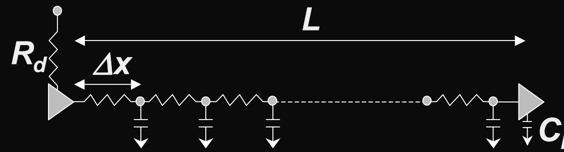
Non-Uniform Temperature-Dependent Delay

- Distributed RC delay model



$$D = R_d (C_L + \int_0^L c_0(x)dx) + \int_0^L r_0(x)(\int_x^L c_0(\eta)d\eta + C_L)dx$$

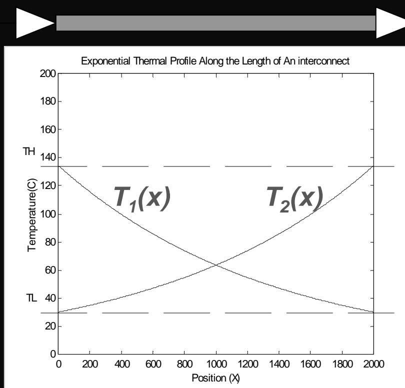
$$D = D_0 + (c_0 L + C_L)\rho_0 \beta \int_0^L T(x)dx - c_0 \rho_0 \beta \int_0^L xT(x)dx$$

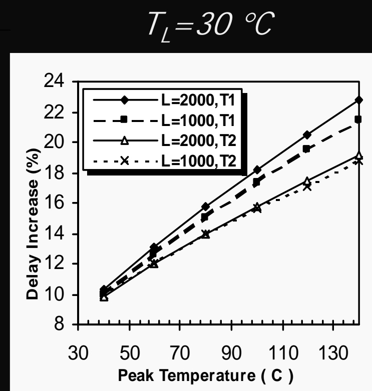
D_0 is the Elmore delay model at 0 °C

Non-Uniform Thermal Effects on Delay Degradation

- Assume two exponential thermal profiles

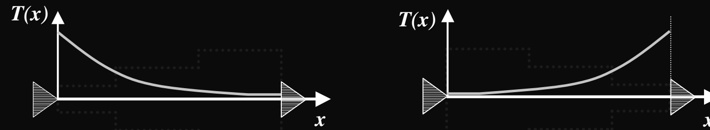
T_L=30 °C





Directional Thermal Profile

- An increasing (decreasing) thermal profile is equivalent to a decreasing (increasing) sizing profile in a uniform resistance wire



- An increasing thermal profile has a better performance than a decreasing thermal profile (optimal wire sizing)

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Clock Net Routing

- Clock is the signal most vulnerable to the underlying thermal non-uniformities
  - Usually driven with the highest average current
  - Has long global segments in the topmost metal layers
- Clock nets must maintain a near-zero skew among their sinks to guarantee the correct functionality of the circuit

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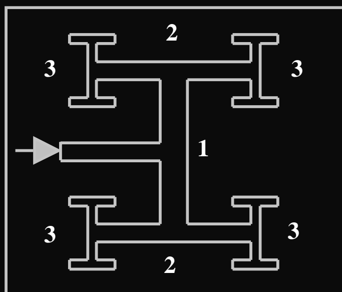
H-Tree Example

- Consider H-Tree clock net



- Balance loads at the merging point in H-Tree to assure zero-skew at two ends of each branch

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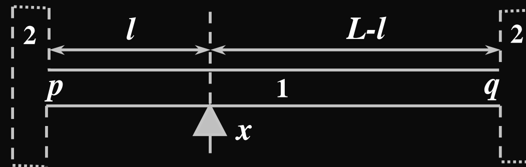
Determining the Branching Point

- With equal load at each endpoint of the wire segment, the branching point is the middle point
- With a non-uniform interconnect thermal profile, the branching point, x , becomes dependent on the thermal profile



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Optimum Location of the Branching Point

- Using the temperature-dependent delay model, the optimal location of the branching point is calculated as:

$$\beta \int_0^{l^*} T(x)\,dx + l^* - A = 0$$

A is a constant

- With a symmetric non-uniform thermal profile, the branching point is still at $l^* = L/2$

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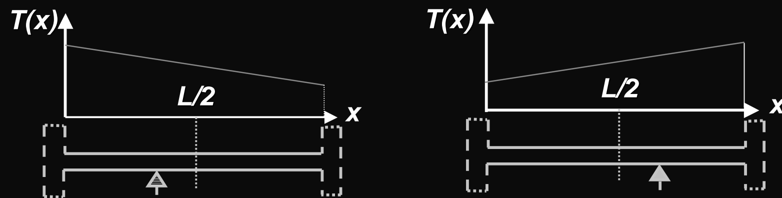
Discussion

- In a gradually decreasing (increasing) thermal profile, optimal length l^* has to be less than (greater than) $L/2$



Experimental Results

$T_{line}(x)$	params	$l = l^*$	$l = L/2$ skew%
$T(x) = ax + b$, $a = \frac{T_H - T_L}{L}$, $b = T_L$	T_H=170, T_L=90	1042	5.42
	T_H=170, T_L=110	1032	3.98
	T_H=170, T_L=130	1021	2.65
$T(x) = a \cdot e^{-bx}$, $b = \frac{1}{L}\ln(\frac{T_H}{T_L})$, $a = T_H$	T_H=170, T_L=90	957.5	5.24
	T_H=170, T_L=110	968.66	3.63
	T_H=170, T_L=130	979.5	2.40
$T(x) = T_{max} \cdot e^{-\frac{(x-\mu)^2}{2\sigma^2}}$	μ=2000, σ=1000	1210	7.78
	μ=1000, σ=400	1000	0.0
	μ=300, σ=700	911	9.57

L=2000 μm

Effects of Non-Uniform Temperature on EDA Tools and Techniques

- Interconnect non-uniform thermal profile can affect many design optimizations:
  - Optimal layer assignment
  - Buffer insertion
  - Wire sizing
  - Gate sizing

Summary

- Peak temperatures in ICs increase with technology scaling in spite of constant power density on dies
- Different switching activities in the substrate give rise to thermal gradients in interconnect lines
- Non-uniformities in the substrate temperature profile greatly impact the interconnect delay
- Such effects were analyzed for a clock tree in the presence of a non-uniform line temperature