

Bounded Algebra and Current-Mode Digital Circuits

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Abstract

This paper proposes two bounded arithmetic operations, which are easily realized with current signals. Based on these two operations, a bounded algebra system suitable for describing current-mode digital circuits is developed and its relationship to the Boolean Algebra, which is suitable for representing voltage-mode digital circuits, is investigated. Design procedure for current-mode circuits using the proposed algebra system is demonstrated on a number of common circuit elements which are used to realize arithmetic operations, such as adders and multipliers.

keywords: Current operation, bounded algebra, current signal, digital circuit

1 Explanation of traditional voltage-mode digital circuit design

The basic tasks of digital circuit design are as follows.

(1) Choose a set of basic operations, which meet two requirements: forming a complete set and being easy to transform in order to express and optimize functions.

(2) Determine an electrical entity from voltage, current or charge to represent the logic signal so as to simplify the realization of the basic operations.

(3) Design various electronic devices corresponding to these basic operations, then realize the given logic function by combining these devices according to the corresponding function expression.

Up until now we always use Boolean algebra to describe the logic function. In the algebra based on comparison lattice, the three basic operations, AND, OR and NOT, can be re-defined as follows:^[1]

$$\text{AND (minimum operation)} \quad x \cdot y \cdot z = \min(x, y, z) \quad (1)$$

$$\text{OR (maximum operation)} \quad x + y + z = \max(x, y, z) \quad (2)$$

$$\text{NOT (threshold comparison)} \quad \bar{x} = \begin{cases} 0, & \text{if } x > 0.5; \\ 1, & \text{if } x < 0.5. \end{cases} \quad (3)$$

In Eq.(3) the detection threshold for signal x is represented by 0.5, which is set in the middle of the two logic levels, 1 and 0. The definition of \bar{x} shows that $\bar{x} = 0$ when $x > 0.5$ (i.e. $x = 1$), and $\bar{x} = 1$ when $x < 0.5$ (i.e. $x = 0$). According to the above definitions all three basic operations in Boolean algebra are related to comparison operation.

It is well known that AND, OR and NOT form a complete set to express arbitrary functions. For example, a function with two inputs can be expressed by the general tabular form as shown in Table 1, where $c_i \in \{0,1\}$. By using these basic operations $f(x,y)$ can be expressed by the following canonical expansion form:

$$f(x, y) = c_0 \cdot (\bar{x} \cdot \bar{y}) + c_1 \cdot (\bar{x} \cdot y) + c_2 \cdot (x \cdot \bar{y}) + c_3 \cdot (x \cdot y) \quad (4)$$

Actually, the above equation describes the procedure to look up Table 1 by using algebraic language. For instance, the first term $c_0 \cdot (\bar{x} \cdot \bar{y})$ in Eq.(4) represents that when $x = 0$ and $y = 0$ the function

value is checked out as c_0 , etc.

Table 1. Tabular expression of 2-input logic function

x	y	$f(x,y)$
0	0	c_0
0	1	c_1
1	0	c_2
1	1	c_3

In the traditional design of digital circuits, voltage is used to represent the logic signal since the voltage signals can easily realize the comparison operations. For example, in bipolar circuits^[2] AND (minimum) and OR (maximum) operations among voltage signals can be realized by pn junction's forward characteristics. On the other hand, in MOS circuits minimum (AND) or maximum (OR) operations among voltage signals can be realized by connecting transistors in series or in parallel, as shown in Fig.1. For instance, the minimum voltage among inputs in Fig.1(a) determines the conduction condition of the series-connected nMOS structure. If $\min(V_x, V_y, V_z)$ is high level (i.e. all inputs are high) the structure will be conductive and the output will be low. (For simplicity, we denote the output by $\overline{\min(V_x, V_y, V_z)}$ in Fig.1(a)). Instead, the maximum voltage among V_x , V_y and V_z determines the conduction condition of the parallel-connected nMOS structure. Obviously, NAND/NOR operations in nMOS circuits are realized based on the structures in Fig.1.(a) and (b), and NOR/ NAND operations in pMOS circuits are realized based on the structures in Fig.1.(c) and (d) (if the positive logic convention is adopted). Besides, combining Fig.1.(a) and 1.(d) will form a NAND gate and combining Fig.1.(b) and 1.(c) will form a NOR gate in CMOS circuits. As to the NOT (threshold comparison) operation, it is realized by comparing the input signal with the inherent threshold voltage of MOS transistors.

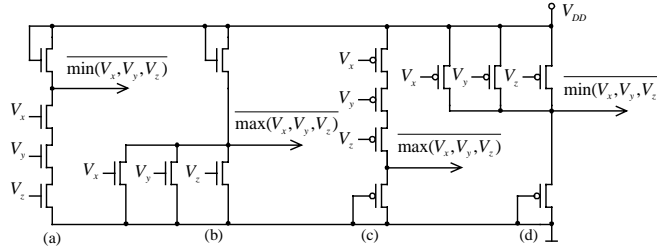


Fig. 1 Comparison of voltage signals by MOS connection

In the previous paragraph, we explained the traditional design of digital circuits by using Boolean algebra and voltage levels. We can now understand why current are seldom used to represent logic signal since it is difficult to compare and select the minimum or maximum among current signals. In the following, we will introduce another kind of operations, which are easy to realize with current signals, and introduce a corresponding algebra for developing the current-mode circuits. This is the main contribution of the present paper.

2 Bounded algebra suitable for current-mode signals

Current is easy to add or subtract by connecting current sources to each other. This indicates to us that if addition (&) and subtraction (-) are introduced as the basic operations their realization based on current signal will be easy. However, the conventional arithmetic addition $x \& y$ and subtraction $x - y$ couldn't be used directly due to complications that $1 \& 1 = 2$ and $0 - 1 = -1$. Instead, we introduce the following two bounded arithmetic operations:

$$\text{Bounded addition} \quad x \uplus y = \min(1, x \& y) = \begin{cases} 1, & \text{if } x \& y > 1; \\ x \& y, & \text{otherwise.} \end{cases} \quad (5)$$

$$\text{Bounded subtraction} \quad x \ominus y = \max(0, x - y) = \begin{cases} 0, & \text{if } x - y < 0; \\ x - y, & \text{otherwise.} \end{cases} \quad (6)$$

We can prove that two bounded operations may be expressed with traditional Boolean operation, AND, OR and NOT, as follows.

$$x \uplus y = x + y \quad (7)$$

$$x \ominus y = x \cdot \bar{y} \quad (8)$$

If $x = 1$ in Eq.(8) we can obtain NOT operation:

$$1 \ominus y = \bar{y} \quad (9)$$

Since OR and NOT form a complete set, therefore, the two bounded operation also form a complete set. In fact the bounded subtraction can form a complete set by itself since $(1 \ominus x) \ominus y = \bar{x} \cdot \bar{y} = x + y$ and NOR forms a complete set. In the next section we will find that the bounded subtraction plays an important role in the design of current-mode circuits.

By using two bounded operations we can express the 2-input functions in Table 1 by the following canonical expansion:

$$f(x, y) = [c_0 \ominus (x \uplus y)] \uplus [c_1 \ominus (x \uplus \bar{y})] \uplus [c_2 \ominus (\bar{x} \uplus y)] \uplus [c_3 \ominus (\bar{x} \uplus \bar{y})] \quad (10)$$

Similarly, the above equation describes the procedure to look up Table 1 by using algebraic expressions. For instance, the first term $c_0 \ominus (x \uplus y)$ in Eq.(10) represents that when $x = 0$ and $y = 0$ the function value is checked out as c_0 , etc. In fact, from Eqs.(7) and (8) we have $c_0 \ominus (x \uplus y) = c_0 \cdot x + y = c_0 \cdot \bar{x} \cdot \bar{y}$. Since the OR operation (+) is equivalent to the bounded addition (\uplus) Eq.(10) is converted into form of Eq.(4).

Based on the above definitions and relationships with Boolean operations, we can derive the following properties for two bounded operations:

$$\begin{aligned} 0 \uplus x &= x, & 1 \uplus x &= 1, & x \uplus x &= x, & x \uplus \bar{x} &= 1; \\ 0 \ominus x &= 0, & 1 \ominus x &= \bar{x}, & x \ominus 0 &= x, & x \ominus 1 &= 0, & x \ominus x &= 0, & x \ominus \bar{x} &= x \end{aligned}$$

Also it may be verified that the above bounded operations have the similar properties with general arithmetic operations, such as:

$$\begin{aligned} x \uplus y &= y \uplus x \\ (x \uplus y) \uplus z &= x \uplus (y \uplus z) = x \uplus y \uplus z \\ x \ominus (y \uplus z) &= (x \ominus y) \ominus z \end{aligned}$$

We should point out that the signal value obtained by the conventional arithmetic addition is restrained by bounding operation with an upper bound 1. In fact, the upper bound may be set to a value d larger than 1, resulting in non-binary signal values. The advantage is that the high valued signal may lead to a simpler function expression and thus a simpler circuit structure. Therefore the

bounded addition operation in Eq.(5) can be modified as

$$x \uplus_d y = \min(d, x \& y) = \begin{cases} d, & \text{if } x \& y > d; \\ x \& y, & \text{otherwise.} \end{cases} \quad (11)$$

where d is a positive integer. If needed the arithmetic addition $\&$ can be directly used for forming an intermediate signal with high value in function expression. As an example, the 3-variable AND and NOR function can be expressed by using the sum signal $\Sigma = x \& y \& z$, $\Sigma \in \{0, 1, 2, 3\}$, as follows:

$$x \cdot y \cdot z = \Sigma \Theta 2 \quad (12)$$

$$\overline{x + y + z} = 1 \Theta \Sigma \quad (13)$$

The above two expressions can be easily verified by using the Karnaugh Map shown in Fig.2.

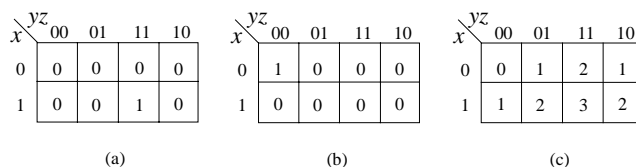


Fig. 2 (a) $x \cdot y \cdot z$ (b) $x + y + z$ (c) $\Sigma = x \& y \& z$

Since the bounded operations are derived from the general arithmetic addition and subtraction, they have simple relationships with traditional Boolean operations. A mediate algebra between arithmetic and Boolean algebra is thus formed.

3 Characteristic of current signals and design of current-mode circuits

CMOS or bipolar technology can be used to illustrate the design of current-mode circuits. I²L is the current-mode circuit in bipolar technology^[3-5]. In this paper only the current-mode circuit in CMOS technology will be discussed since it is receiving increasing attention in recent years^[6-10].

The circuit realizations of the two bounded operations are shown in Fig.3(a). In the left part the current flowing through the connection node cannot be larger than 1, therefore, the bounded addition is realized. On the other hand, in the right part the current flowing through the connection node cannot be less than 0, then the bounded subtraction is realized. Notice that its load is an nMOS current mirror. In the following we show examples of building current-mode digital circuits.

(1) Inverter

From Eq.(9) we can obtain a simple circuit realization shown in the left part of Fig.3(b), where only two nMOS transistors (for the current mirror) and one pMOS transistor (for forming the current source 1) are used. The dotted line in the circuit is used to express the control of a current mirror. The shortcoming of this realization is lack of level-restoration. However, based on Eq.(3) we can design an inverter with level-restoration function, as shown in the right part of Fig.3(b). Here node P assumes a high level, nMOS transistor turns off and output current is 0 when $x = 1$ (i.e. $x > 0.5$); Similarly node P assumes low level, pMOS transistor turns on and output current is 1 when $x = 0$ (i.e. $x < 0.5$). In Fig.3(b) two pMOS transistors and one nMOS transistor are needed. One of pMOS transistors is used to switch the unit current source.

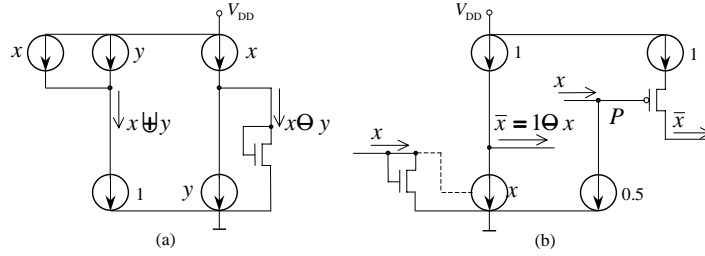


Fig. 3 (a) Circuit realization of bounded operations (b) Current-mode inverter

(2) Boolean logic gates

From Eqs.(12) and (13), the simple AND and NOR gates without level-restoration function are shown in Fig.4(a) and (b), where the intermediate sum signal $\Sigma = x \& y \& z$ is used. Instead, we can derive the following switching expressions from Karnaugh Map in Fig.2:

$$x \cdot y \cdot z = \begin{cases} 0, & \text{if } \Sigma < 2.5; \\ 1, & \text{if } \Sigma > 2.5. \end{cases}$$

$$\overline{x \cdot y \cdot z} = \begin{cases} 0, & \text{if } \Sigma > 2.5; \\ 1, & \text{if } \Sigma < 2.5. \end{cases}$$

$$x + y + z = \begin{cases} 0, & \text{if } \Sigma < 0.5; \\ 1, & \text{if } \Sigma > 0.5. \end{cases}$$

$$\overline{x + y + z} = \begin{cases} 0, & \text{if } \Sigma > 0.5; \\ 1, & \text{if } \Sigma < 0.5. \end{cases}$$

The corresponding current-mode Boolean gates with restoration function are shown in Fig.4(c), (d), (e) and (f).

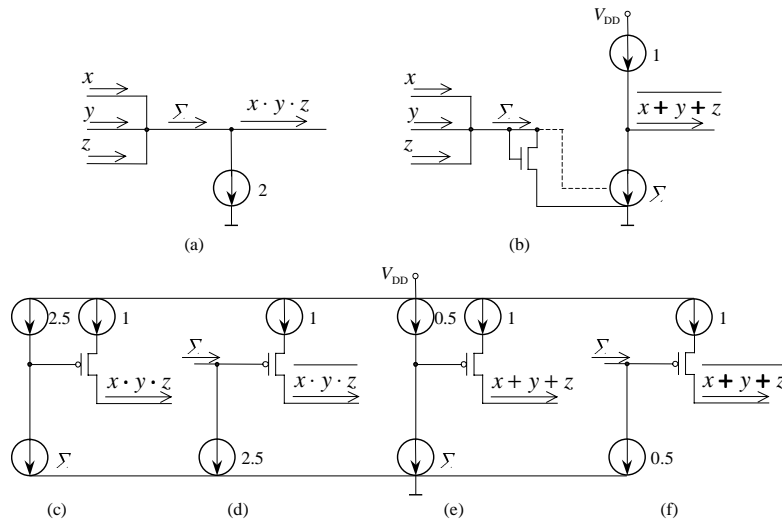


Fig. 4 Current-mode Boolean gates (a) simple AND gate (b) simple NOR gate (c) AND gate (d) NAND gate (e) OR gate (g) NOR gate

(3) Arithmetic circuits

Since currents are easy to add or subtract, the current-mode circuit is most suitable for realizing arithmetic circuits such as adders and multipliers. Taking the full adder with three inputs (A, B, C) and two outputs (carry-out C_+ and sum S) as the example, we can obtain Table 2 by using the intermediate sum signal $\Sigma = x \oplus y \oplus z$ and derive the following switching expressions for C_+ and S :

$$C_+ = \begin{cases} 0, & \text{if } \Sigma < 1.5; \\ 1, & \text{if } \Sigma > 1.5. \end{cases}$$

$$S = \begin{cases} 0, & \text{if } \Sigma < (2C_+ \& 0.5); \\ 1, & \text{if } \Sigma > (2C_+ \& 0.5). \end{cases}$$

Table 2. Truthtable of a full adder

Σ	0	1	2	3
C_+	0	0	1	1
S	0	1	0	1

Notice that in the function S the switching threshold is controlled by carry-out C_+ . The corresponding circuit realizations are shown in Fig.5(a), where three nMOS transistors are used for forming the current mirror of Σ , five pMOS transistors with various widths are used for generating the five current sources (1.5, 1, 2, 0.5, 1), and other three pMOS transistors are used as switches. Therefore, a total of 11 MOS transistors are needed for the current-mode full adder. In contrast, the voltage-mode full adder needs 28 MOS transistors for a full complementary MOS realization^[11]. If we do not use C_+ to control switch threshold in design we can derive S directly from its truthtable given in Table 2:

$$S = \begin{cases} 1, & \text{if } (\Sigma > 0.5 \text{ and } \Sigma < 1.5) \text{ or } \Sigma > 2.5; \\ 0, & \text{otherwise.} \end{cases}$$

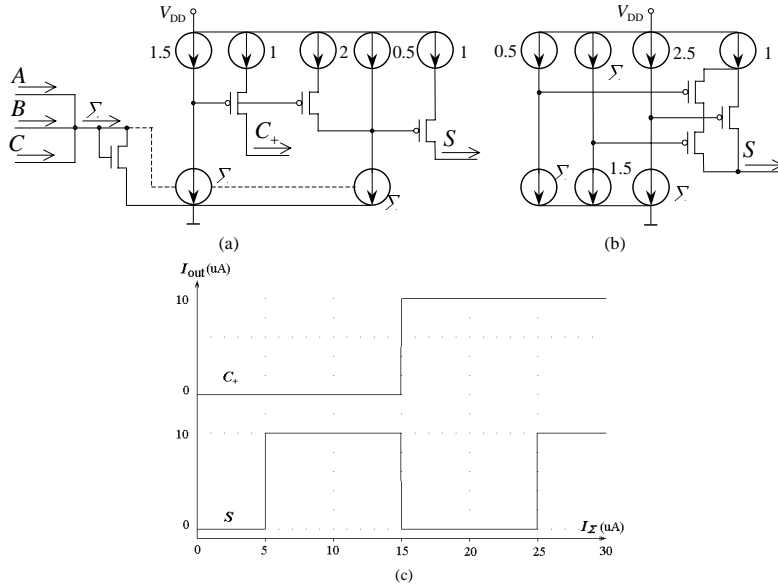


Fig. 5 Current-mode full adder and its DC transfer characteristics

The design corresponding to the above switching expression is shown in Fig.5(b). PSPICE has been used to simulate the circuit in Fig.5(a) with $1\mu m$ CMOS technology. The currents corresponding to logic level 0, 1, 2, 3 are 0, $10\mu A$, $20\mu A$ and $30\mu A$, respectively. The DC transfer characteristics of the

circuit is given in Fig.5(c). It is shown that the circuit has ideal logic function with precise detective threshold currents corresponding to 0.5 (5 μ A), 1.5 (15 μ A) and 2.5 (25 μ A).

In fact the higher the number of signals which are added together, the higher the area advantage of current-mode circuits. For example, four adders will be needed to realize addition of seven binary signals in voltage-mode design, as shown in Fig.6(a). This realization needs 112 transistors. However, in current-mode design, we can derive the following expressions from the truth table shown in Table 3:

$$y_2 = \begin{cases} 0, & \text{if } \Sigma < 3.5; \\ 1, & \text{if } \Sigma > 3.5. \end{cases}$$

$$y_1 = \begin{cases} 0, & \text{if } \Sigma < (4y_2 \& 1.5); \\ 1, & \text{if } \Sigma > (4y_2 \& 1.5). \end{cases}$$

$$y_0 = \begin{cases} 0, & \text{if } \Sigma < (4y_2 \& 2y_1 \& 0.5); \\ 1, & \text{if } \Sigma > (4y_2 \& 2y_1 \& 0.5). \end{cases}$$

The circuit corresponding to the above expressions is shown in Fig.6(b), where only 19 MOS transistors are used. It is thus evident that devices and interconnections will be significantly reduced in arithmetic circuits, such as adder and multiplier, if current-mode design are used. The most convincing demonstration of the advantages of current-mode CMOS design is a 32 \times 32 multiplier presented^[6]. This 32 \times 32 multiplier chip is half the size of an equivalent voltage-mode CMOS realization, dissipates half the power, and has a multiply time within 5% of the fastest reported multiply time of a comparable design of that era.

Table 3. Truth table of a seven binary signals.

S	0	1	2	3	4	5	6	7
y_2	0	0	0	0	1	1	1	1
y_1	0	0	1	1	0	0	1	1
y_0	0	1	0	1	0	1	0	1

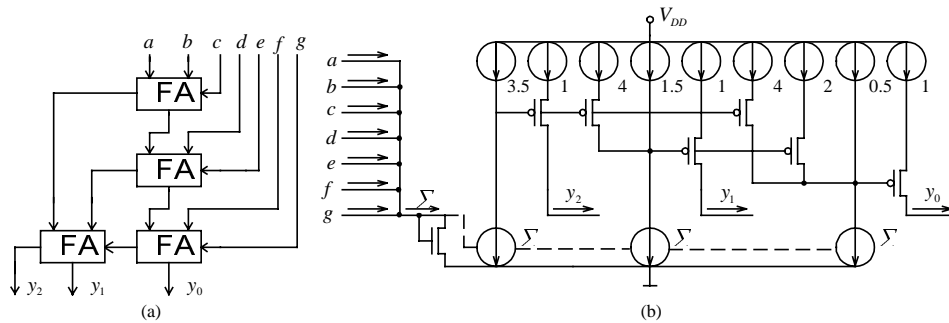


Fig. 6 Adder of seven binary signals (a) voltage-mode (b) current-mode

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4 Conclusions

This paper showed that the choice of algebra system used for designing digital circuits is dependent on which electrical entity is used to represent the logic signal in circuits. If the voltage signal is used, the Boolean algebra based on comparison lattice is a better choice. However, if the current signal is used, comparison operations in Boolean algebra are not easy to realize. Since addition or subtraction operations can be easily realized by connecting wires together, we introduced bounded arithmetic operations as the basic operations and formed a corresponding bounded algebra suitable for the design of current-mode circuits. The design procedure of the current-mode circuits was demonstrated for some typical circuits. It was shown that the proposed bounded operations and the corresponding algebra system are very effective for designing current-mode circuits. In addition to the design flexibility, the arithmetic circuits, such as adders and multipliers, have simple structure in current-mode realization. In the end, as the charge signal and current signal are all easy to be added, we should point out that the bounded algebra can be spreaded into charge circuits, such as CCD.^[12]

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