Battery-Powered Digital CMOS Design

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Abstract — *In this paper, we consider the problem of maximizing the battery life (or duration of service) in battery-powered CMOS circuits. We first show that the battery efficiency (or utilization factor) decreases as the average discharge current from the battery increases. The implication is that the battery life is a super-linear function of the average discharge current. Next we show that even if the average discharge current remains the same, different discharge current profiles (distributions) may result in very different battery lifetimes. In particular, the maximum battery life is achieved when the variance of the discharge current distribution is minimized. Analytical derivations and experimental results underline the importance of the correct modeling of the battery-hardware system as a whole and provide a more accurate basis (i.e., the battery discharge times delay product) for comparing various low power optimization methodologies and techniques targeted toward battery-powered electronics. Finally, we calculate the optimal value of V_{dd} for a battery-powered VLSI circuit so as minimize the product of the battery discharge times circuit delay.*

I. INTRODUCTION

With the rapid progress in the semiconductor technology, the chip density and operation frequency have largely increased, making the power consumption in digital circuits a major concern for VLSI designers. High power consumption reduces the battery life in portable devices. Therefore, the goal of low-power design for battery-powered devices is to extend the battery lifetime while meeting the performance requirement.

An effective method for low-power design is to reduce the supply voltage while maintaining the performance using a combination of architectural and circuit optimization techniques. In general, for a fixed supply voltage level, low power techniques target at reducing the average current drawn by the circuit [6]. Voltage scaling techniques on the other hand, scale the supply voltage to reduce power dissipation. These techniques can be divided into *static voltage scaling* [1][2] and *dynamic voltage scaling* [3]. The effectiveness of these techniques can be evaluated by using appropriate metrics, such as power, energy, delay, or energy-delay product. These metrics can be used in different applications (depending on the design requirements) to guide optimization toward the best solution. It has been argued in [2] that the energy-delay product is more relevant for comparing of various low power design methodologies and techniques.
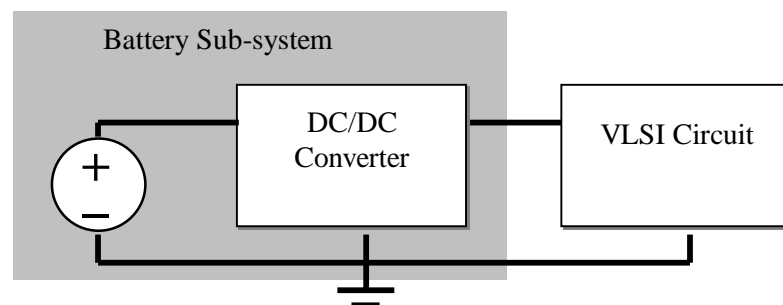
Figure 1 An integrated model of battery-powered system

As shown in Figure 1, a battery-powered digital system (which is typically present in portable electronic devices such as cellular phones, notebook computers, PDA's) consists of the VLSI circuit, the battery cell, and the DC/DC converter. Despite the fact that low-power design for portable electronics targets at extending the battery life, discussions of low-power-design metrics and methodologies have entirely focused on the VLSI circuit itself, assuming that the battery sub-system is an ideal source that outputs a constant voltage and stores/delivers a fixed amount of energy [4]. However, in reality, the energy stored in a battery may not be extracted orused to the full extent. In some situations, even 50% energy delivery is not possible. This phenomenon is caused by the fact that the "actual capacity" of the battery depends strongly on the mean value and the profile (distribution) of the current discharged from the battery. More precisely, a higher portion of the battery capacity is wasted at a higher

discharge current. High rate (current) discharge can indeed cause dramatic (more than 40%) waste of the initial capacity (energy storage) of the battery [5]. Furthermore, even for the same mean value of discharge current, the battery efficiency may change by as much as 25% as a result of the discharge current profile over time.

We will show that, for a given battery, the amount of energy that can be used by the VLSI circuit is a function of the current discharge rate of the VLSI circuit. The battery life does not have a simple linear relationship with the power consumption of the circuit. For example, a 2X increase in circuit power consumption may cause a 3X reduction in the battery lifetime, compared with the 2X reduction in the ideal case. Therefore, we argue that for portable battery-powered electronics, the appropriate metric to guide various design optimizations is the *battery discharge - delay product*, and not simply the energy-delay product [2]. In addition, we will show that because of the dependence of battery capacity on discharge current, current discharge with same average value but different profiles (distributions) will lead to different battery lifetimes.

Analytical derivations and experimental results demonstrate that correct modeling of the battery-hardware system as a whole can provide a more accurate basis for comparing various low power optimization methodologies and techniques targeted toward battery-powered electronics.

This paper is organized as follows: Section II provides the background, Section III gives an analysis of the relationship between the current profile and the battery life, Section IV considers the problem of optimal supply voltage selection, Sections V provides the experimental results and VI presents our conclusions.

II.   BACKGROUND

A.   *Battery Overview*

Many different types of batteries are being used in a wide range of applications [5]-[15]. They can be divided into the *primary batteries* (non-rechargeable) and the *secondary batteries* (rechargeable). Batteries can also be classified based on the electrochemical material used for their electrodes or the type of their electrolytes, e.g., Lead-acid, Ni-Cd, Ni-Zn, Ag-Zn, Zn-Air, Nickel-Metal Hydride, Lithium-Ion, Lithium-Polymer, etc. Among

these, the Nickel-Metal Hydride battery and the Lithium-Ion battery are currently the most popular batteries for portable electronic devices, ranging from cellular phones to notebook computers.

Figure 2 shows the internal structure of a typical rechargeable lithium battery. It consists of the lithium foil anode, the composite cathode, and the electrolyte that serves as an ionic path between electrodes and separates the two materials. Electrical energy is generated by chemical reaction among these three components. For rechargeable batteries, applying electrical recharging can reverse the chemical reaction; hence the battery can be used for multiple times (normally several hundred times).
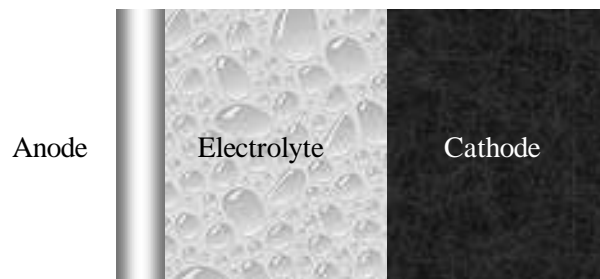

Figure 2 The internal structure of a Lithium battery
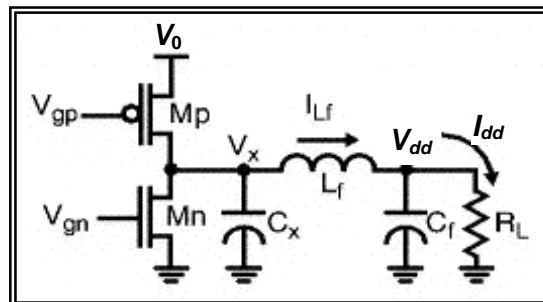
B.   DC/DC Converters

Figure 3 The Buck Converter of a DC/DC converter

Figure 3 (taken from [5]) shows the block diagram the Buck Converter of a high-efficiency DC/DC converter that can be integrated on the chip. **The control circuit of the DC/DC converter is not shown here for saving space.** Node V_0 is the input of the DC/DC converter that is connected to the positive electrode of the battery. Node V_{dd} is

the output of the DC/DC converter that is connected to the VLSI circuit. The control circuit is used to adaptively generate the switching signals for the Buck Converter such that the voltage at V_{dd} is stabilized at the target supply voltage for the VLSI circuit.

If we define η as the conversion efficiency of the DC/DC converter, we have:

$$\eta \cdot V_0 \cdot I_0 = V_{dd} \cdot I_{dd} \tag{2.1}$$

where I_0 and I_{dd} are average input and output current of the DC/DC converter over some period of time. V_0 and V_{dd} are similarly defined. Notice that V_0 and I_0 are also the output voltage and current of the battery, V_{dd} and I_{dd} are also the supply voltage and current for the VLSI circuit.

C.   Battery Capacity and Efficiency

One important characteristics of the battery is that some amount of energy will be wasted when the battery is delivering the energy required by the circuit [7]-[16]. In analytical form, given a fixed battery output voltage, if the circuit current requirement for the battery is I, the actual current that is taken out of the battery is:

$$I^{act} = \frac{I}{\mu}, \quad 0 \le \mu \le 1 \tag{2.2}$$

where μ is called the battery efficiency (or utilization) factor. I^{act} is always larger than or equal to I.

Defining CAP_0 as the amount of energy that is stored in a new (or fully charged) battery and CAP^{act} as the actual energy that can be used by the circuit, Eqn. (2.2) is equivalent to:

$$CAP^{act} = CAP_0 \cdot \mu, \quad 0 \le \mu \le 1 \tag{2.3}$$

The efficiency factor μ is a function of discharge current I:

$$\mu = f(I) \tag{2.4}$$

where *f* is a monotonic-decreasing function [5]. Only the low-frequency part of the current is relevant to changing the battery efficiency [15]. Therefore, *I* must be the average output current of the battery over certain amount of time, which can be represented as *N·T*, where *N* is some positive integer and *T* is the clock cycle. *N·T* may be as large as a few seconds [15]. The actual capacity of the battery decreases when the discharge current increases.
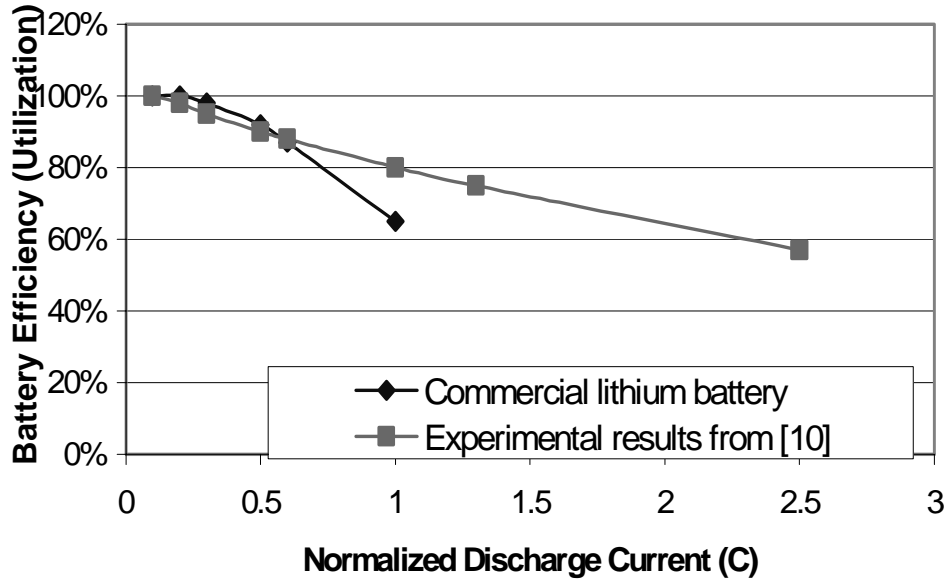

Figure 4 Discharge capacity of a commercial lithium battery

Figure 4 shows the efficiency factor versus discharge current curves extracted from the data sheet of a commercial Lithium battery [16] and the experimental results from [11]. Similar curves exist for other lithium batteries [7][8][14] and for NiMH batteries [13][14].

To obtain an analytical form for the discussions in the remainder of the paper, two simple functions are used to approximate the battery efficiency factor:

$$\mu = 1 - \beta \cdot I \tag{2.5}$$

or

$$\mu = 1 - \gamma \cdot I^2 \tag{2.6}$$

where β and γ area positive constant numbers.

In our experience, either Eqn. (2.5) or Eqn. (2.6) provide good modeling for the capacity-current relation of Lithium batteries as long as the appropriate value of β or γ is chosen.

D. *Notation*

The following notations are used in our analytical results:

T: Clock cycle time for one operation

V_0: Output voltage of the battery

I_0: Average output current of the battery over time $N{\cdot}T$

V_{dd}: Supply voltage of the circuit

I_{dd}: Average supply current of the circuit over time $N{\cdot}T$

μ: Efficiency factor of the battery

η: Efficiency of the DC/DC converter

P^{ide}: Ideal battery power required by the circuit

P^{act}: Actual battery power needed for output power of P

E^{ide}: Ideal energy needed to complete an operation

E^{act}: Actual battery energy needed to complete an operation

CAP_0: Total energy stored in a new battery

DOS: Duration of service, or battery lifetime, equals to CPA_0 divided by P^{act}.

BD: Battery discharge.

Notice that V_0, V_{dd} and η are nearly constant during the circuit operation.

III. CURRENT PROFILE VERSUS DURATION OF SERVICE

We will show that, even with the same power consumption, the battery lifetime is different for different circuit current profile (also referred to as the current distribution).

Assume that, during the circuit operation, the magnitude of the average circuit current[2] I_{dd} follows a certain probability density function $p_1(I_{dd})$, and the battery current I_0 follows the density function $p_2(I_0)$. From Eqn. (2.1) we know that p_1 and p_2 have a linear relationship, the only difference is the scales of the axes. Therefore, we will focus on the relation between p_2 and the battery life; our derivations are equally applicable to p_1.

A. *Actual power and duration of service*

Let I_0^{ave} be the mean value of distribution $p_2(I_0)$, we can write the **ideal** power consumption of the circuit as:

$$P^{ide} = \int_{I_{0,MIN}}^{I_{0,MAX}} V_0 \cdot I_0 \cdot p_2(I_0)dI_0 = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} I_0 \cdot p_2(I_0)dI_0 = V_0 \cdot I_0^{ave}$$

The **actual** power consumption of the circuit can be written as:

$$P^{act} = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} \frac{I_0}{\mu(I_0)} \cdot p_2(I_0)dI_0 \tag{3.1}$$

If we substitute μ using Eqn. (2.5), Eqn. (3.1) becomes:

$$P^{act} = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} \frac{I_0}{1 - \beta \cdot I_0} \cdot p_2(I_0)dI_0 \tag{3.2}$$

Under the constraint of a fixed mean value I_0^{ave}, it is easy to prove that the maximum P^{act} occurs when I_0 follows a uniform distribution, i.e.,

$$p_2(I_0) = \begin{cases} \dfrac{1}{I_{0,MAX} - I_{0,MIN}}, & I_{0,MIN} \le I_0 \le I_{0,MAX} \\ 0, & otherwise \end{cases} \tag{3.3}$$

The minimum P^{act} occurs when I_0 follows a Dirac's δ-function distribution, i.e.,

$$p_2(I_0) = \delta(I_0 - I_0^{ave}) \tag{3.4}$$

Substituting (3.3) and (3.4) into (3.2) respectively, we obtain:

$$P_{MAX}^{act} = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} \frac{I_0}{1 - \beta \cdot I_0} \cdot \frac{1}{(I_{0,MAX} - I_{0,MIN})} dI_0 = \frac{V_0}{(I_{0,MAX} - I_{0,MIN})} \cdot \frac{\beta(I_{0,MIN} - I_{0,MAX}) + \ln(\frac{1 - \beta \cdot I_{0,MIN}}{1 - \beta \cdot I_{0,MAX}})}{\beta^2}$$

and $$P_{MIN}^{act} = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} \frac{I_0}{1 - \beta \cdot I_0} \cdot \delta(I_0 - I_0^{ave}) dI_0 = \frac{V_0 \cdot I_0^{ave}}{1 - \beta \cdot I_0^{ave}}$$ (3.5)

If we use Eqn. (2.6) instead, Eqn. (3.1) can be written as:

$$P^{act} = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} \frac{I_0}{1 - \gamma \cdot I_0^2} \cdot p_2(I_0) dI_0$$ (3.6)

and we obtain the following expressions for the maximum and minimum P^{act}:

$$P_{MAX}^{act} = \frac{V_0}{(I_{0,MAX} - I_{0,MIN})} \cdot \frac{\ln(\frac{1 - \gamma \cdot I_{0,MIN}^2}{1 - \gamma \cdot I_{0,MAX}^2})}{2\gamma} \quad \text{and} \quad P_{MIN}^{act} = \frac{V_0 \cdot I_0^{ave}}{1 - \gamma \cdot (I_0^{ave})^2}$$ (3.7)

B. Quantitative example

To get a more intuitive view, we assign $V_0=4V$, $I_{0,MIN}=0$, $I_{0,MAX}=5A$, $\beta=0.12$, $\gamma=0.024$, and $CAP_0=36KJ$ (2.5 Amp-Hour at 4.0V output voltage). Notice that the values of β and γ are chosen such that both (2.5) and (2.6) evaluate to 0 when $I_o=0$ and evaluate to 0.4 when $I_o=5A$. Figure 5 and Figure 6 give several simple distributions with the same mean value of 2.5A for the discharge current[3]. The current profiles in Figure 5 are representative of the current profile for a circuit, which is operating, in one stable mode (uni-modal operation). The current profiles in Figure 6 are representative of the current profile for a circuit, which is operating alternatively between two stable modes (bi-modal operation). The phenomenon of bi-modal operation may be caused by input characteristics of the circuit, the scheduling of the tasks, or dynamic power management. Table 1 and

Table 2 give the corresponding duration-of-service when using Eqn.(2.5) and Eqn. (2.6) for μ.

From the results in Table 1 and

Table 2, we make the following conclusions:

1. The maximum *DOS* occurs by using the δ-function distribution whereas the minimum *DOS* occurs by using the uniform distribution. There is a significant increase (20%-30%) in *DOS* from the worst case to the best case.

2. With *δ*-function current distribution, a circuit with bi-modal current distribution exhausts the battery more rapidly compared to one with the same average current but a uni-modal operation. The opposite is true for uniform uni-modal versus bi-modal current distributions.

3. The variation of *DOS* from best case to worst case current profile is much higher for the uni-modal operation compared with the bi-modal operation.
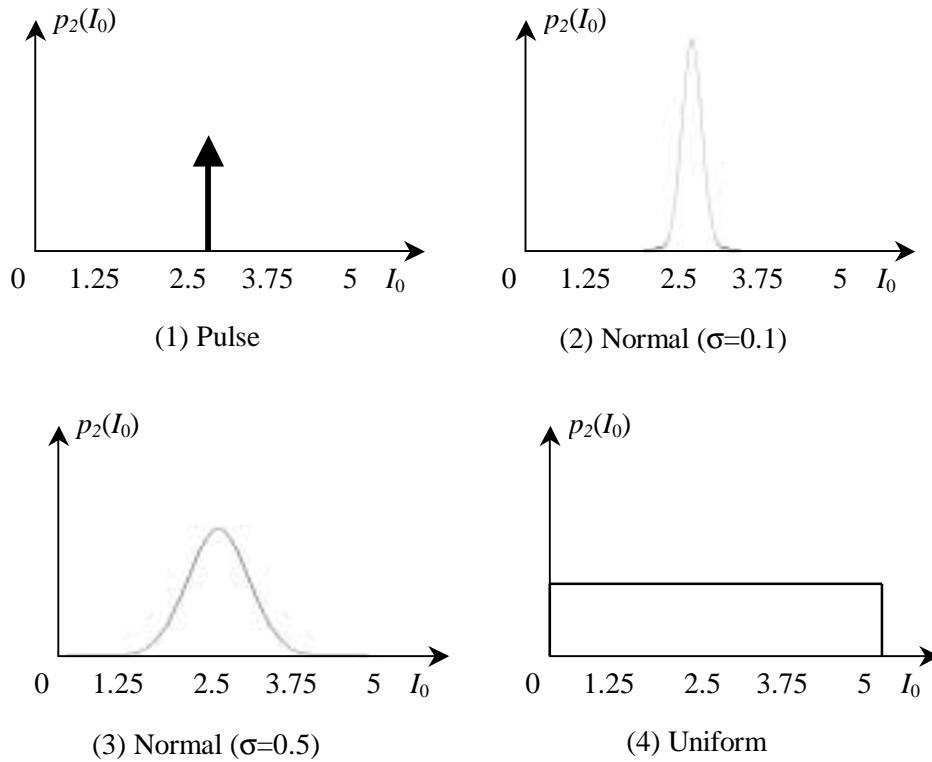

(1) Pulse

(2) Normal (σ=0.1)

(3) Normal (σ=0.5)

(4) Uniform

Figure 5 Current profiles for uni-modal operation

(1)

(2)

(3)

(4)
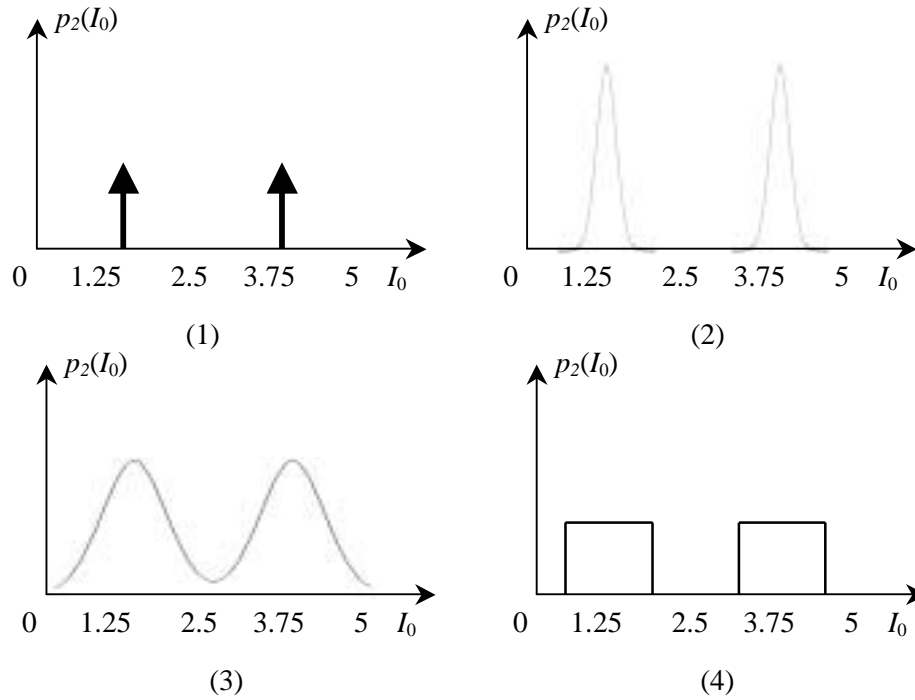
Figure 6 Current profiles for bi-modal operation

Table 1 Battery lifetime for uni-modal current profile

Profile		1	2	3	4
DOS (hour)	Eqn. (2.5) with β=0.12	0.70	0.70	0.68	0.57
	Eqn. (2.6) with γ=0.024	0.85	0.85	0.83	0.65

Table 2 Battery lifetime for bi-modal current profile

Profile		1	2	3	4
DOS (hour)	Eqn. (2.5) with β=0.12	0.60	0.60	0.59	0.59
	Eqn. (2.6) with γ=0.024	0.72	0.72	0.70	0.70

IV. MINIMIZING THE PRODUCT OF BATTERY-DISCHARGE AND DELAY

In the past, the energy-delay metric was used to find an optimal supply voltage V_{dd} for the best power-performance tradeoff. Here we propose another metric for low power design in an integrated battery-hardware model, the ***battery discharge*-delay product**. This metric is similar to the energy-delay product while accounting for the battery characteristics and the DC/DC conversion efficiency. The *BD*-delay product states that the design goal should be to minimize delay and maximize battery lifetime at the same time.

The problem of static voltage scaling for a battery-power system is defined as: Given a battery with certain characteristics, a DC/DC converter with certain efficiency, and a design of CMOS circuit, find the optimal supply voltage V_{dd} for the CMOS circuit such that the *BD*-delay product is minimized.

A. The BD-delay product

We define the **Battery Discharge** (*BD*) as:

$$BD = \frac{E^{act}}{CAP_0} \tag{4.1}$$

As we discussed in previous section, E^{act} will be different for different current profiles. For convenience of presentation, we assume that the current distribution follows the simplest (and best) profile i.e., a δ-function distribution as shown in Fig. 5.(1). Obviously, other current distributions could be used instead. Therefore, we have:

$$BD = \frac{E^{act}}{CAP_0} = \frac{V_0 \cdot I_0 \cdot T}{CAP_0 \cdot \mu(I_0)} \tag{4.2}$$

The ideal energy needed for circuit to complete an operation is [2]:

$$E^{ide} = V_{dd} \cdot I_{dd} \cdot T = \tfrac{1}{2} C_{sw} \cdot V_{dd}^2 \tag{4.3}$$

where C_{sw} is the total switched capacitance during the operation.

From Equations (2.1), (4.2) and (4.3), we can write BD as a function of V_{dd}:

$$BD = \frac{C_{sw}}{2 \cdot \eta \cdot CAP_0} \cdot \frac{V_{dd}^2}{\mu(k \cdot V_{dd}^2 / T)} \tag{4.4}$$

where $k = C_{sw}/(2 \cdot \mu \cdot V_0)$.

Either (2.5) or (2.6) can substitute the efficiency function μ in (4.4). Without loss of generality, we only use (2.5) for the rest of our discussion.

Substituting (2.5) in (4.4), we obtain:

$$BD = \frac{C_{sw}}{2 \cdot \eta \cdot CAP_0} \cdot \frac{V_{dd}^2}{(1 - \beta \cdot k \cdot V_{dd}^2 / T)} \tag{4.5}$$

For today's deep sub-micron CMOS technology, the delay of a circuit can be modeled as:

$$t_d = m \frac{V_{dd}}{(V_{dd} - V_{th})^\alpha}, \qquad 1 < \alpha \le 2 \tag{4.6}$$

where m is some constant and V_{th} is the threshold voltage of the transistor. Notice that Eqn. (4.6) can be used for modeling the delay of the whole circuit, as well as a single gate.

We can thus write the *BD*-delay (*BD-D*) product as:

$$BD\text{-}D = \frac{m \cdot C_{sw}}{2 \cdot \eta \cdot CAP_0} \cdot \frac{V_{dd}^3}{(1 - \beta \cdot k \cdot V_{dd}^2 / T) \cdot (V_{dd} - V_{th})^\alpha} \tag{4.7}$$

When we are calculating the optimal V_{dd} that minimizes the *BD-D* product, we need to consider two different cases on *T*:

1. **Fixed operation latency**: *T* is constant for all V_{dd} values. In this case, Eqn. (4.7) can be used to calculate the optimal V_{dd}.

2. **Variable operation latency**: T changes when V_{dd} changes. In this case, it is reasonable to assume that T is proportional to operation delay:

$$T \propto t_d \Rightarrow T = m' \frac{V_{dd}}{(V_{dd} - V_{th})^\alpha}, \qquad 1 < \alpha \le 2$$

Therefore, the *BD-D* product is written as:

$$BD\text{-}D = \frac{m \cdot C_{sw}}{2 \cdot \eta \cdot CAP_0} \cdot \frac{V_{dd}^3}{(1 - \beta \cdot k \cdot V_{dd} \cdot (V_{dd} - V_{th})^\alpha / m') \cdot (V_{dd} - V_{th})^\alpha} \qquad (4.8)$$

We will see in the next section, although the optimal V_{dd} values calculated by (4.7) and (4.8) are different, they have similar characteristics.

B.   *Quantitative examples*
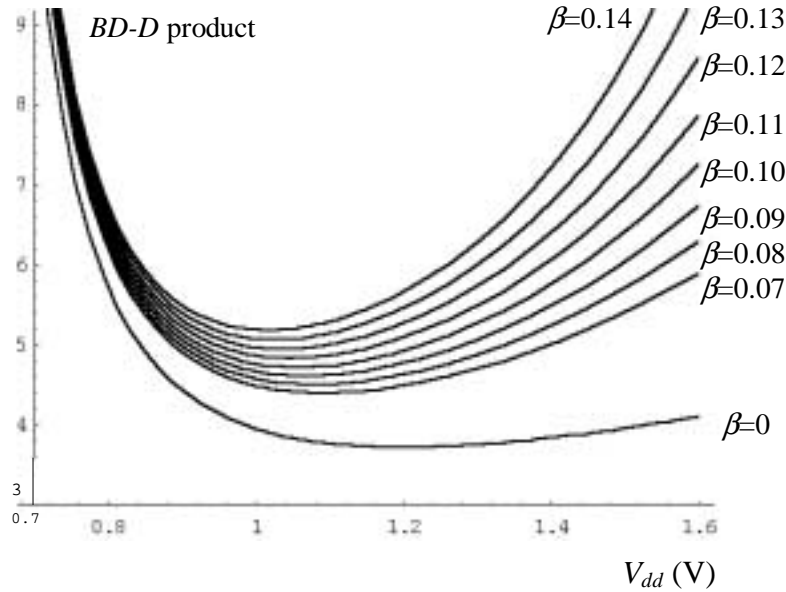
1. Fixed Operation Latency (FOL)

BD-D product

$\beta = 0.14$ $\beta = 0.13$
$\beta = 0.12$
$\beta = 0.11$
$\beta = 0.10$
$\beta = 0.09$
$\beta = 0.08$
$\beta = 0.07$

$\beta = 0$

V_{dd} (V)

Figure 7 *BD-D* product curves with different β values (FOL)

Assume a VLSI circuit consumes 13.5W power at supply voltage of V_{dd}=1.5V. Let V_0=4V and η=0.9. We have k/T=1.7. Let α=1.5, and V_{th}=0.6V. We normalized $(m \cdot C_{sw})/(2 \cdot \eta \cdot CAP_0)$=1 since their values will not influence the optimal V_{dd} and the shape of BD-D product. To show the influence of the battery characteristics on the optimal V_{dd}, we use β values of (0, 0.07, 0.08, 0.09, 0.1, 0.11, 0.12, 0.13, 0.14) to generate a group of BD-D product curves and compare the optimal V_{dd} values. Notice that if β=0, the BD-D product is equivalent to the ideal case where the energy-delay product is calculated without considering the battery characteristics. Figure 7 shows the plot of BD-D product curves with different β values. Table 3 shows the corresponding optimal V_{dd} values.

Table 3 Optimal V_{dd} for minimum BD-D product (FOL)

β	0	0.08	0.09	0.10	0.11	0.12	0.13	0.14
Optimal V_{dd} (V)	1.200	1.080	1.068	1.057	1.047	1.037	1.027	1.018

2. Variable Operation Latency (VOL)

The parameter settings are same as in the case of fixed operation latency, except that k/m' (instead of k/T) is calculated to be 3.0. Figure 8 shows the plot of BD-D product curves with different β values. Table 4 shows the corresponding optimal V_{dd} values.

Table 4 Optimal V_{dd} for minimum BD-D product (VOL)

β	0	0.08	0.09	0.10	0.11	0.12	0.13	0.14
Optimal V_{dd} (V)	1.200	1.073	1.063	1.054	1.046	1.038	1.031	1.024

The results in Tables 3 and 4 show that the optimal V_{dd} for minimum BD-D product in an integrated battery-hardware model can differ by about 10% to 15% from the one which does not consider the battery characteristics. The optimal V_{dd} will decrease when β increases.
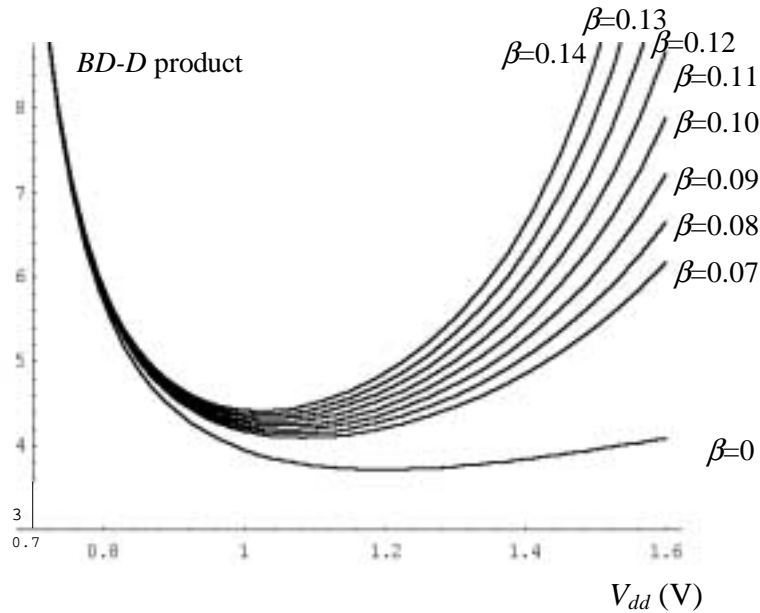
Figure 8 *BD-D* product curves with different β values (VOL)

V. EXPERIMENTAL RESULTS

Experiments using HSPICE simulation are designed to verify our analysis in previous sections.

A macro-model of the battery was generated following the model proposed by [15]. The parameters in the macro-model were set according to the data sheet of a commercial lithium battery [16]. The capacity of the battery is 3 Amp-Hour and the output voltage is 3.8V. The capacity-current characteristic of the battery has been shown in Figure 4. $N \cdot T$ is set to be 6 seconds.

An appropriate macro-model was used for the DC/DC converter simulation. The efficiency of the converter was set to 90% for converting V_0 to different V_{dd}'s.

Seven different profiles for the battery discharge current are generated. They are:

1) δ-function distribution with mean of 1.5A

2) Normal distribution with mean of 1.5A and $\sigma = 0.1$

3) Normal distribution with mean of 1.5A and $\sigma = 0.5$

4) Uniform distribution over region [0, 3]

5) Bi-modal δ-function distributions with means of 0.25A and 2.75A for each mode

6) Bi-modal δ-function distributions with means of 0.5A and 2.5A for each mode

7) Bi-modal δ-function distributions with means of 1A and 2A for each mode

The simulated duration of service (or battery lifetime) for different current profiles are reported in Table 5. The experimental results are consistent with our analysis.

Table 5 Simulation results of *DOS* for different profiles

Profile	1	2	3	4	5	6	7
DOS (hours)	1.77	1.72	1.49	1.42	1.46	1.52	1.64

For the experimental setup of the *BD*-delay product (variable operation latency), we designed a small system where the VLSI circuit is represented by an optimally sized 4-inverter buffer with a capacitive load of 0.5pF. A 0.35µ CMOS process technology (BSIM3 models) [17] is used for the transistor models. Several supply voltages ranging from 0.8V to 1.6V are used for the buffer. For each supply voltage, delay and average current are measured for the buffer to make a single transition. The delay values are directly used in the final *BD*-delay product. We scale-up the average current by a factor of 15,000 to create a more realistic discharge current profile representative of a VLSI circuit. We then use the average current as the battery discharge current to get the values of *BD*. The simulated *BD-D* product curve is shown in Figure 9. For the battery model used, the simulated optimal V_{dd} value for minimum *BD-D* product is 0.9V.
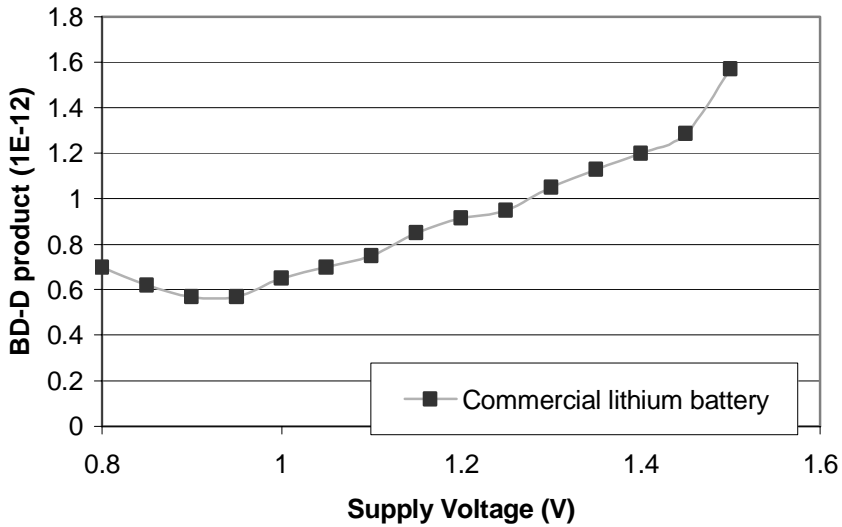
Figure 9 Experimental results of the *BD-D* product curve

From our experiments and analysis, we drew the following implications for low power design of battery-powered devices:

1. Current profile has a significant impact on the duration of service of the battery. When designing or optimizing a circuit for low power, both the average current dissipation and the variance of the average current must be considered.

2. The incorporation of real battery characteristics in the low power design analysis necessitates the use of even lower supply voltages by pushing the optimal V_{dd} (for minimum *BD-D* product) lower than was initially thought [2]. Using an integrated battery-hardware model, , achieving higher circuit performance by increasing the supply voltage level is even costlier than previously thought.

VI.   CONCLUSION

In this paper, we showed that it is essential to consider the characteristics of the battery that powers a portable electronic circuit in deciding the effectiveness of various low power optimization techniques. We also proposed a

simple, yet accurate, integrated model of the battery and VLSI sub-systems. We then studied the relationship between battery lifetime and different current distributions. Next we studied the problem of assigning a voltage level to the VLSI circuit that minimizes the product of delay and the battery discharge in the combined system. Finally we give some suggestions for low power design for battery-powered devices.

REFERENCES

[1] A. Chandrakasan, R. Brodersen, *Low Power Digital CMOS Design*, Kluwer Academic Publishers, July 1995.

[2] M. Horowitz, T. Indermaur, and R. Gonzalez, "Low-Power Digital Design", *IEEE Symposium on Low Power Electronics*, pp.8-11, 1994.

[3] A. Chandrakasan, V. Gutnik, and T. Xanthopoulos, "Data Driven Signal Processing: An Approach for Energy Efficient Computing", *1996 International Symposium on Low Power Electronics and Design"*, pp. 347-352, Aug. 1996.

[4] J. Rabaey and M. Pedram, *Low Power Design Methodologies*, Kluwer Academic Publishers, 1996

[5] URL: http://infopad.eecs.berkeley.edu/~anthonys/quals

[6] M. Pedram, "Power Minimization in IC Design: Principles and Applications", *ACM transactions on Design Automation of Electronic Systems*, Vol. 1, No. 1, pp. 3-56, Jan., 1996.

[7] M. Doyle, T. F. Fuller, and J. Newman, "Modeling of Galvanostatic Charge and Discharge of the Lithium/Polymer/Insertion Cell", *J. Electrochem. Soc.*, Vol. 140, No. 6, pp.1526-1533, Jun. 1993.

[8] T. F. Fuller, M. Doyle, and J. Newman, "Simulation and Optimization of the Dual Lithium Ion Insertion Cell", *J. Electrochem. Soc.*, Vol. 141, No. 1, pp.1-9, Jan. 1994.

[9] D. Fauteux, "Lithium Polymer Electrolyte Rechargeable Battery", *The Electrochemical Society Proceedings*, Vol. 94-28, pp.379-388.

[10]   L. Xie, W. Ebner, D. Fouchard, and S. Megahed, "Electrochemical Studies of $LiNiO_2$ for Lithium-Ion Batteries", *The Electrochemical Society Proceedings*, Vol. 94-28, pp.263-276.

[11]   K. M. Abraham, D. M. Pasquariello, T. H. Nguyen, Z. Jiang, and D. Peramunage, "Lithiated Manganese Oxide Cathodes for Rechargeable Lithium Batteries", *The Battery Conference*, pp. 317-323, 1996.

[12]   N. Cui, B. Luan, D. Bradhurst, H. K. Liu, and S. X. Dou, "Surface-Modified Mg_2Ni-Type Negative Electrode Materials for Ni-MH Battery", *The Battery Conference*, pp. 317-322, 1997.

[13]   J. K. Erbacher and S. P. Vukson, "Commercial Nickel-Metal Hydride (Ni-MH) Technology Evaluation", *The Battery Conference*, pp. 9-15, 1997

[14]   B. Nelson, "TMP Ultra-High Rate Discharge Performance", *The Battery Conference*, pp. 139-143, 1997.

[15]   S. Gold, "A PSPICE Macromodel for Lithium-Ion Batteries", *The Battery Conference*, pp. 215-222, 1997

[16]   URL: http://www.valence-tech.com/products/index.htm

[17]   URL: http://www.mosis.org/html/hp-gmos10qa-prm.html