

An accurate analytical I - V model for sub-90-nm MOSFETs and its application to read SNM modeling

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Abstract: In this work, first an accurate model for I - V characteristics of sub-90-nm MOSFET in the linear and saturation regions is proposed. The model, which is intended for fast analytical calculation of the current, is based on the BSIM3v3 model. Instead of using constant V_{th} and V_A voltages, as is assumed in the BSIM3v3 model, these voltages are defined as functions of the gate-source voltage. The accuracy of the model is verified by comparing its results with those of HSPICE for the 90, 65, 45, and 32 nm CMOS technologies. The model shows better accuracy than the n^{th} -power and BSIM3v3 models. Then, we use the proposed I - V model to calculate the read static noise margin (SNM) of nano-scale conventional 6T SRAM cells with high accuracy. The read SNM is calculated by approximating the inverter transfer voltage characteristic of the cell in the regions where vertices of the maximum square of the butterfly curves are placed. The results for the SNM are also in excellent agreement with those of the HSPICE simulation for 90, 65, 45, and 32 nm technology nodes. The validity of the model is also verified in the presence of process variations and negative bias temperature instability (NBTI). Finally, it is shown that the model can accurately predict the minimum supply voltage required for a target yield.

Key words: Modeling, Nano-scale, Process variation, Read SNM, SRAM

1 Introduction

Analytical I - V models are necessary for the design of integrated circuits. In the nano-scale regime, a simple square law model for the I - V characteristics of MOSFETs is inaccurate primarily because of velocity saturation and short channel effects. There have been many attempts to accurately model the characteristics of these transistors, including complicated empirical models used for HSPICE simulations. Simple models preserving high accuracy have also been developed for circuit analysis. The n^{th} -power model (Sakurai and Newton, 1990; Sakurai and Newton, 1991), which assumes a non-integer n^{th} -power relation between current and voltage, is an example of these models. The model has been recently modified for sub 65 nanometer technologies (Hiroki *et al.*, 2008). Whilst the model speeds up simulations, obtaining analytical circuit parameters such as stability metrics of SRAM cells requires the use of circuit models with integer powers between current and voltage in order to provide explicit rather than implicit expressions for these metrics.

SRAM robustness in the hold and read states is measured by using Static Noise Margin (SNM) as the figure of merit. The SNM is in turn defined as the DC-voltage disturbance that takes the SRAM cell to the edge of instability (Lohstroh *et al.*, 1983). In (Lohstroh *et al.*, 1983), different equivalent criteria for the definition of SNM have been presented. They include small signal closed loop gain of cross coupled inverters of the SRAM cell, and the side length of the maximum square between the normal and mirrored voltage transfer characteristics. In (Seevinck *et al.*, 1987), an analytical SNM model, based on the square law device current equation, is proposed. Since the law is not valid for sub-90 nanometer technology, the model may not be used in this regime. In (Bhavanagarwala *et al.*, 2001), an SNM model using the trans-regional drain current model (Bhavanagarwala *et al.*, 2000) is presented. The model is implicit and complex, relying on fixed point iterations to obtain

self-consistency. In (Chen *et al.*, 2007), the voltage transfer characteristics of the cross coupled inverters of an SRAM cell have been estimated as a Butterworth filter. The error of this technique was less than 8%. In this case, however, no closed form expression for the SNM was derived. In addition, it was assumed that all of the transistor threshold voltages have the same magnitude. In (Agarwal and Nassif, 2008), the small signal closed loop gain of cross coupled inverters of SRAM cell was used as a criterion for the SNM modeling. This model was based on simulation where process variation effects could not be investigated readily. The SNM modeling for sub-threshold SRAM also has been examined in (Calhoun and Chandrakasan, 2006; Hu *et al.*, 2009).

This paper has two contributions. First, a model for the *I-V* characteristics of sub-90-nm is proposed. The key advantage of the proposed model compared to the existing models is its ability to analytically model the *I-V* characteristics of highly scaled transistors with very good accuracy. The existing analytical models for *I-V* characteristics of highly scaled CMOS technologies are either too complex with too many parameters which prohibits their use for hand calculations (e.g., numerical models used in HSPICE) or they are too simplistic with very low accuracies (such as the α -power law or the n^{th} -power law.) Second, as an example of the effectiveness of the proposed model, we use it to analytically obtain SNM of SRAMs with higher accuracy than the previous analytical models. The rest of the paper is organized as follows. In Section 2, the *I-V* model for the bulk MOSFET is described. The modeling of the read SNM is described in Section 3 while the results are discussed in Section 4. Finally, Section 5 concludes the paper.

2 Proposed *I-V* model

To obtain expressions for the SNM parameter of the SRAM cell, we need expressions for the *I-V* characteristics of the transistors in both the linear and saturations regions. In this work, we propose a simple *I-V* model which can be used for the SNM calculations.

2.1 Linear region

Our model is based on the BSIM3v3 model for hand calculations. The BSIM3v3 model equation in the linear region ($V_{ds} \leq V_{dsat}$) is given by (Cheng *et al.*, 1995)

$$I_{ds} = \mu_{\text{eff}} C_{ox} \frac{W}{L} \frac{1}{1 + \frac{V_{ds}}{E_{sat} L}} (V_{gs} - V_{th} - \frac{V_{ds}}{2}) V_{ds} \quad (1)$$

$$V_{dsat} = \frac{E_{sat} L (V_{gs} - V_{th})}{E_{sat} L + V_{gs} - V_{th}} \quad (2)$$

where μ_{eff} is the effective mobility, C_{ox} is the gate capacitance per unit area, W is the channel width, L is the channel length, V_{ds} is the drain-source voltage, V_{gs} is the gate-source voltage, V_{th} is the threshold voltage, and E_{sat} is the minimum electric field for the onset of velocity saturation. In the BSIM3v3 model, for V_{th} we utilized the effective threshold voltage specified by the technology (Morshed *et al.*, 2009). In our proposed model, we use the same equations as above except that we replace V_{th} by a fitted threshold voltage which is a function of V_{gs} (see below). Using this approach, we achieve both simplicity and accuracy in our calculations.

The current-voltage characteristics obtained from the HSPICE simulations, the BSIM3v3 model Eq. (1), the n^{th} -power law, and the proposed model for a 45nm technology are plotted in Fig. 1. We used the BSIM4 technology model for our HSPICE simulations (Morshed *et al.*, 2009). The fitting parameters of the n^{th} -power model were determined by the procedure discussed in (Sakurai and Newton, 1991). As shown in the figure, the results of the BSIM3v3 model deviates considerably from those of the HSPICE simulations. While the n^{th} -power model has good accuracy at the bias points where the fitting parameters were determined, its error becomes non-negligible at other bias points.

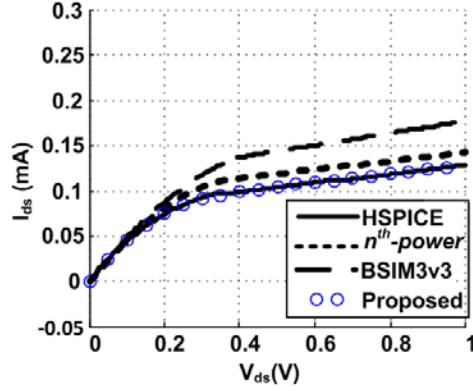


Fig. 1 I_{ds} - V_{ds} characteristics calculated by HSPICE simulations, n^{th} -power, BSIM3v3 and proposed models at $V_{gs} = 0.9$ V for 45 nm technology

We explain how the (fitted) threshold voltage is determined in the proposed model. Fig. 2 depicts the threshold voltage of the model, denoted by V_{th} , versus V_{gs} for the 32 nm, 45 nm, 65 nm, and 90 nm technologies (Morshed *et al.*, 2009). Next, we model V_{th} as a function of V_{gs} . The V_{th} is determined such that the error of the proposed model compared to the HSPICE results is minimized. As seen from the results, we can divide the characteristics into two regions determined by a point (V_{thl}). Based on the observations, we propose the following expressions for modeling the V_{th} - V_{gs} characteristic

$$V_{th} = \begin{cases} -a_1(V_{gs} - V_{thl})^2 + V_{thl0} & V_{gs} \leq V_{thl} \\ -a_2(V_{gs} - V_{thl})^2 + V_{thl0} & V_{gs} > V_{thl} \end{cases} \quad (3)$$

where V_{thl0} is the *fitted* threshold voltage for V_{gs} equal to V_{thl} , a_1 and a_2 are two model parameters. Later, we will explain how to compute these parameters. Our results for the four technologies shown in Fig. 2 demonstrate that V_{thl} is the *technology threshold voltage* (denoted as V_{th0} in HSPICE). For example, in the 45nm technology, V_{thl} is equal to 0.466 V. To determine whether the modeling remains valid if the technology uses other threshold voltage values, we altered the technology threshold voltage (V_{th0} in HSPICE) between 0.37 V and 0.55 V in the 45 nm technology model. The simulations results again revealed the same characteristics for V_{th} versus V_{gs} and very good accuracy for the proposed model (Fig. 3). It should be noted that the modeling results for PMOS transistors are similar in terms of their accuracy.

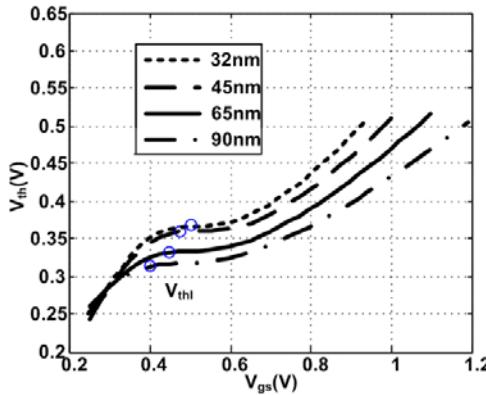


Fig. 2 V_{th} - V_{gs} characteristics for 32, 45, 65, and 90 nm technologies

The long channel threshold voltage is given by (Tsividis, 2003)

$$V_{thl} = V_{FB} + 2\phi_f + \frac{Q_{dep}}{C_{ox}} + \frac{Q_{im}}{C_{ox}} \quad (4)$$

where V_{FB} is the flat band voltage, ϕ_f is the energy of the Fermi level in the bulk with respect to the intrinsic level, Q_{dep} is the depletion charge, Q_{im} is the implant dose ($\#/cm^2$) and C_{ox} is the oxide capacitance per cm^2 .

Using the results shown in Fig. 3, we obtain the V_{thl0} - V_{thl} characteristics which are shown in Fig. 4.

The data reveals a linear relationship between V_{thl0} and V_{thl} as

$$V_{thl} - V_{thl0} = d \quad (5)$$

where values of d are 0.13, 0.11, 0.09, and 0.08 for the 32 nm, 45 nm, 65 nm, and 90 nm, respectively. These values suggest that as the channel length increases, V_{thl0} becomes closer to V_{thl} .

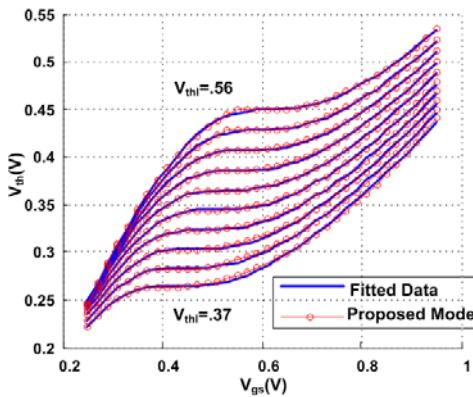


Fig. 3 V_{th} - V_{gs} characteristics for 45 nm technology with V_{thl} as the running parameter

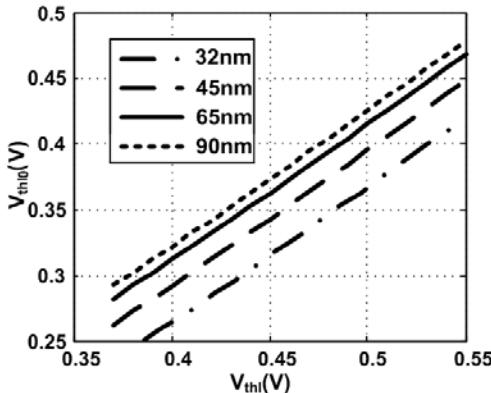


Fig. 4 V_{thl0} - V_{th} characteristics for 32, 45, 65 and 90 nm technologies

As the next step, to find simple expressions for the minimum of V_{gs} which turns the transistor *on*, it is necessary to model the V_{gseff} ($= V_{gs} - V_{th}$) versus V_{gs} characteristic. Our proposed expressions for this characteristic are presented for two different cases of V_{gs} smaller and larger than V_{thl} :

Case 1: $V_{gs} \leq V_{thl}$,

$$V_{gseff} = V_{gs} - V_{th} =$$

$$a_1[V_{gs} - (V_{thl} - \frac{1}{2a_1})]^2 - \frac{1}{4a_1} + V_{thl} - V_{thl0} \quad (6)$$

As shown in Fig. 5, V_{gseff} becomes zero when the slope of the curves, dV_{gseff}/dV_{gs} , is zero. Thus, in the above equation, the sum of the last three terms on the right hand side must be equal to zero. From this, it is possible to write

$$a_1 = \frac{1}{4(V_{thl} - V_{thl0})} \quad (7)$$

and

$$V_{gseff} = a_1[V_{gs} - b_1]^2 \quad (8)$$

where, b_1 is the V_{gs} at the onset of transistor conduction, *i.e.*, the effective threshold voltage, and is given by

$$b_1 = V_{thl} - \frac{1}{2a_1} = 2V_{thl0} - V_{thl} \quad (9)$$

The values of a_1 obtained from fitting the results of Fig. 5 also verify this analysis. Note that for this case, the transistor conducts when V_{gs} is larger than b_1 . As the channel length increases, V_{thl0} approaches V_{thl} making a_1 very large and b_1 very close to V_{thl} . Therefore, for long channel transistors, the conducting region $b_1 < V_{gs} \leq V_{thl}$ vanishes and we only have *on* current for $V_{gs} > V_{thl}$.

Case 2: $V_{gs} > V_{thl}$

$$V_{gseff} = a_2[V_{gs} - b_2]^2 + c_2 \quad (10)$$

where

$$b_2 = (V_{thl} - \frac{1}{2a_2}) \quad (11)$$

$$c_2 = -\frac{1}{4a_2} + V_{thl} - V_{thl0} \quad (12)$$

Our simulations show that a_2 also depends on V_{thl} . By inspecting Fig. 2, we find that the slope of V_{th} versus V_{gs} for $V_{gs} > V_{thl}$ becomes smaller as the channel length increases and a_2 approaches zero implying a weak dependence of V_{th} on V_{gs} .

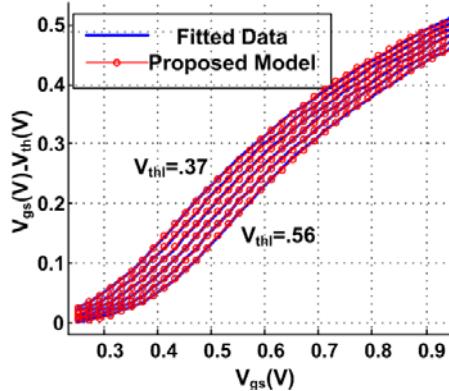


Fig. 5 (V_{gs} - V_{th}) versus V_{gs} characteristics for the 45 nm technology with V_{thl} as the running parameter

2.2 Saturation region

In the saturation region ($V_{ds} > V_{dsat}$), using BSIM3v3 model, the current-voltage characteristics may be expressed as (Cheng *et al.*, 1995)

$$I_{ds} = I_{dsat} \left(1 + \frac{V_{ds} - V_{dsat}}{V_A}\right) \quad (13)$$

where I_{dsat} is the saturation current, V_{dsat} was defined in Eq. (2), and V_A is the voltage for modeling the drain induced barrier lowering effect in the saturation region. In this work, similar to modeling V_{th} as a function of V_{gs}

in the linear region, we propose to model the V_A as a function of V_{gs} in the saturation region using

$$V_A = \begin{cases} V_{As1}(V_{gs} - V_{th}) - \frac{V_{dsat}}{2} & V_{gs} \leq V_{th} \\ V_{As2}V_{gs} + V_{Ah} & V_{gs} > V_{th} \end{cases} \quad (14)$$

where V_{As1} , V_{As2} , and V_{Ah} are fitting parameters. Fig. 6 shows a comparison between V_A predicted by our model and the one obtained from the HSPICE simulation results. The comparison shows very high accuracy for the model.

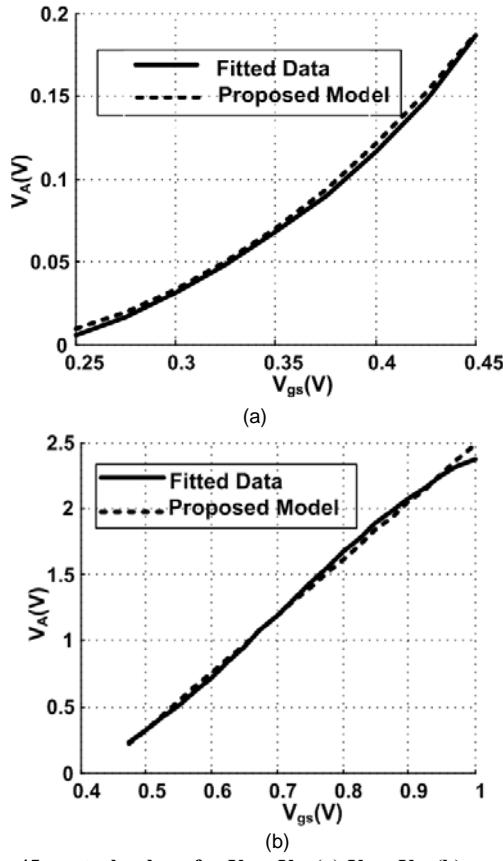


Fig. 6 V_A - V_{gs} characteristics for the 45 nm technology for $V_{gs} \leq V_{th}$ (a) $V_{gs} > V_{th}$ (b)

In Fig. 7, the I_{ds} - V_{ds} characteristics with V_{gs} as the running parameter are depicted for the 45 nm technology. As observed, the results of the proposed model closely match the HSPICE results for wide ranges of V_{gs} and V_{ds} . To quantify this, we used multipoint Percent Mean Absolute Deviation (PMAD) between the actual and predicted curves (Chiulli, 1999). For calculating the PMAD values, the absolute value of the difference between the actual and predicted values of data is divided by the actual value for every data point. Then, the results for all data points are added and divided by the number of data points (Chiulli, 1999). The total PMAD for all the regions is 1.8% for the 45 nm technology. As will be seen later, this high accuracy helps us in accurately modeling the read SNM. The PMAD values for different regions are also listed in Table 1. It shows that the PMAD values for $V_{gs} > V_{th}$ are very low while they are rather high for $V_{gs} \leq V_{th}$. The reason that they are larger for $V_{gs} \leq V_{th}$ is that the current amplitude is low in this (narrow) region. This error will not have a major impact on the accuracy of the read SNM modeling.

Finally, it should be mentioned that the body effect as well as the temperature and process variation effects

may be incorporated in the model. For this purpose, existing formulas in the literature which model these effects may be included in the model. Also, note that our simulation results show that in the presence of typical variations the changes in the model parameters are negligible (see Section 4). By typical variations, we mean that the changes of the parameter are within, typically, 20% (e.g., in the case of threshold voltage) of its nominal value. The variations correspond to three times of the standard deviation.

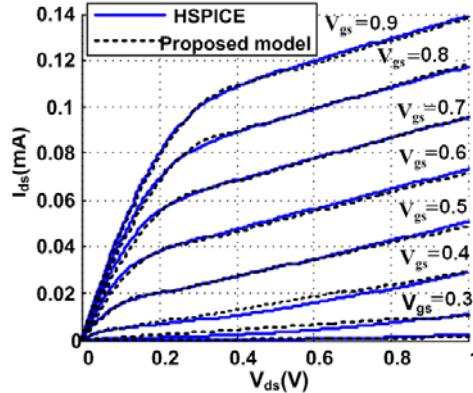


Fig. 7 I_{ds} - V_{ds} characteristic for 45 nm technology using our proposed model

Table 1 PMAD values for different region of I_{ds} - V_{ds} characteristic for the 45 nm technology

Region	PMAD
$V_{GS} \leq V_{THL}$	$V_{ds} \leq V_{dsat}$ 9.9%
$V_{THL} < V_{GS} \leq V_{ds}$	$V_{ds} > V_{dsat}$ 23.6%
$V_{GS} > V_{THL}$	$V_{ds} \leq V_{dsat}$ 1.7%
	$V_{ds} > V_{dsat}$ 1.2%

2.3 Parameter extraction

The model parameters may be extracted by choosing the sample points shown on the I - V curves of Fig. 8. Substituting the expression for V_{gseff} given by Eq. (8) into Eq. (1) and considering that V_{ds} is the same for points 1, 2, and 3, b_1 can be found as

$$b_1 = \frac{\frac{V_{gs1}^2 - V_{gs2}^2}{I_1 - I_2} - \frac{V_{gs1}^2 - V_{gs3}^2}{I_1 - I_3}}{2\left(\frac{V_{gs1} - V_{gs2}}{I_1 - I_2} - \frac{V_{gs1} - V_{gs3}}{I_1 - I_3}\right)} \quad (15)$$

Similarly, by substituting expression for V_{gs} - V_{th} given by Eq. (10) into Eq. (1) and considering that V_{ds} is the same for points 1, 4, and 5, b_2 can be obtained as

$$b_2 = \frac{\frac{V_{gs1}^2 - V_{gs4}^2}{I_1 - I_4} - \frac{V_{gs1}^2 - V_{gs5}^2}{I_1 - I_5}}{2\left(\frac{V_{gs1} - V_{gs4}}{I_1 - I_4} - \frac{V_{gs1} - V_{gs5}}{I_1 - I_5}\right)} \quad (16)$$

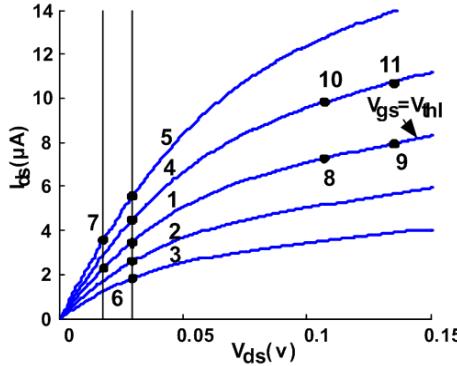


Fig. 8 Sample points on I_{ds} - V_{ds} Characteristic for extraction of parameters

After finding b_1 and b_2 , we can find V_{thl0} and a_2 from Eqs. (9) and (11), respectively. Next, a_1 can be computed from Eq. (7). The parameter values for $\mu_{eff}C_{ox}W/L$ and $E_{sat}L$ can also be found from the technology file for the given technology. To increase the accuracy, the values of these parameters may, however, be computed from the I - V curves of Fig. 8. Noting that the values of V_{gs} and V_{th} for points 5 and 7 in this figure are the same and using Eq. (1), one may find the first parameter as

$$\frac{1}{2}\mu_{eff}C_{ox}\frac{W}{L} = \frac{I_5\left(\frac{1}{V_{ds5}} + \frac{1}{E_{sat}L}\right) - I_7\left(\frac{1}{V_{ds7}} + \frac{1}{E_{sat}L}\right)}{V_{ds5} - V_{ds7}} \quad (17)$$

Similarly, note that the values of V_{gs} and V_{th} for points 5 and 7 as well as 1 and 6 are the same and also the values of V_{ds} are equal for points 1 and 5 as well as 6 and 7. Using Eq. (1), we determine the second parameter as

$$E_{sat}L = \frac{(I_1 - I_5) - (I_6 - I_7)}{\frac{I_1 - I_5}{V_{ds1}} - \frac{I_6 - I_7}{V_{ds6}}} \quad (18)$$

For obtaining V_{As1} , we choose points 8 and 9 which have the same V_{gs} ($V_{gs} = V_{thl}$). Using Eqs. (13) and (14), we may write

$$V_{As1} = \mu_{eff}C_{ox}\frac{W}{L} \times \frac{V_{ds8} - V_{ds9}}{I_8 - I_9} \times \frac{\frac{V_{dsat8}}{V_{dsat8} + E_{sat}L}}{E_{sat}L} \quad (19)$$

For calculating V_{As2} , we consider points 8, 9, 10, and 11. Note that since the values of V_{gs} and V_{thl} are equal for points 10 and 11 as well as points 8 and 9, the corresponding values of V_{dsat} are also equal. Using Eqs. (13) and (14), together with the fact that the values of V_{ds} at points 8 and 10 as well 9 and 11 are equal, it is possible to write

$$V_{As2} = \frac{I_{dsat8} \times \frac{V_{ds8} - V_{ds9}}{I_8 - I_9} - I_{dsat10} \times \frac{V_{ds10} - V_{ds11}}{I_{10} - I_{11}}}{V_{gs8} - V_{gs10}} \quad (20)$$

Finally, V_{Ah} may be computed from the continuity condition of V_A defined by Eq. (14) when V_{gs} is equal to V_{thl} .

It is imperative to mention that only b_1 , b_2 , V_{As1} , and V_{As2} are extracted from the I - V characteristics for each technology. All other parameters are either obtained from these parameters or from the technology file. Finally, the flowchart for obtaining the drain current as a function of gate and drain voltages is illustrated in Fig. 9.

3 Read SNM calculation

In this section, we use the analytical model obtained for the $I-V$ characteristic of the transistor in deriving expressions for the read SNM of a 6T SRAM cell which is shown in Fig. 10.

As shown in Fig. 11, for calculating the read SNM, the control signals of WL , BL , and BLC must be set to V_{dd} and a voltage source should be applied to VL to obtain the DC transfer characteristic (the main curve shown by the solid line in Fig. 12). Using Fig. 12, which shows VR versus VL , four different regions are specified. In region 1, AR is off and NR is in the saturation region with V_{gs} less than V_{thh} while PR is in the linear region with V_{sg} more than $|V_{thlp}|$.

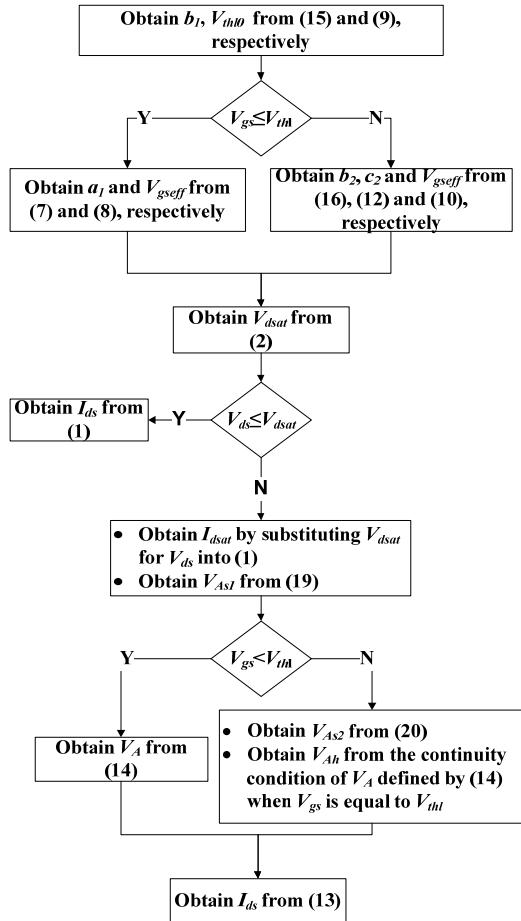


Fig. 9 Flowchart for obtaining I_d for given V_{gs} and V_d

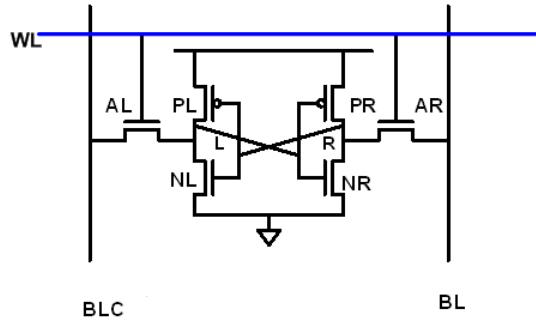


Fig. 10 A conventional 6T SRAM cell

In regions 3 and 4, NR is in the linear mode with V_{gs} more than V_{thln} , while AR is in the saturation region with V_{gs} greater than V_{thln} . PR is in the saturation region with V_{sg} less than $|V_{thlp}|$ in region 3 and is off in region 4. We must also have the other DC transfer

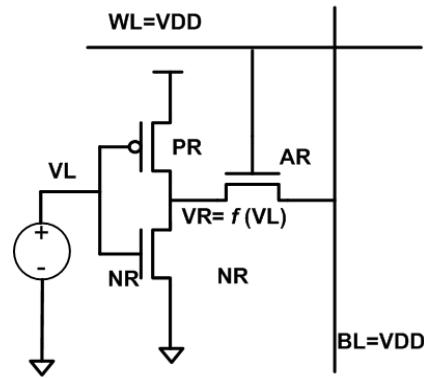


Fig. 11 SRAM Cell configuration for calculating forward dc transfer characteristics ($VR = f(VL)$) for read SNM calculation

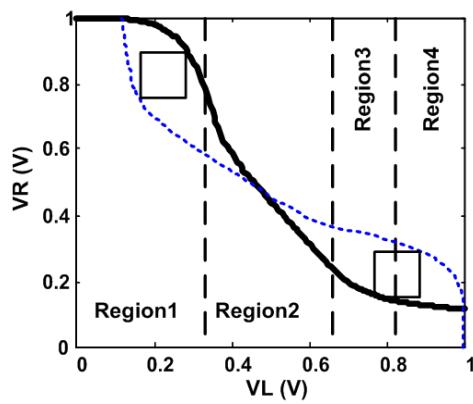


Fig. 12 Butterfly curve in the read mode

characteristic which is the mirror of the main characteristic. This curve is obtained in the same way except that a voltage source is applied to VR this time (the mirrored curve is shown by the dashed line in Fig. 12).

SNM may be calculated from the maximum side length of the square whose vertices lie on the curves. As shown in Fig. 12, there are two such squares. For the asymmetric case in which the left and right transistors are not the same, the minimum side length is considered as SNM. Here, we show how to calculate the maximum

side length of the left square and that the right one can be easily found by exchanging the corresponding right and left values in the final expression of SNM. For the left square, one of the vertices is in region 1 of the main curve and the other is in region 3 or 4 of the mirrored curve as shown in Fig. 12. Thus, to make the calculation easier, it is better to find VL versus VR in regions 3 and 4. Also, note that since none of the vertices of the maximum square encompassing in the butterfly curves is placed in region 2, we are not concerned about the operational modes of the transistors in this region. This assumption holds true in the presence of process variations (see, e.g., (Bhavanagarwala *et al.*, 2001; Kang *et al.*, 2007)).

In fact, the intersection of the two characteristics forming the butterfly characteristic plot (see Fig. 12), which occurs in region 2, is a function of the ratios of the threshold voltages of the left and right NMOS/PMOS transistors. Changes in the ratios due to the variations only partially shift region 2 (including the intersection) to the left or right in the butterfly characteristic plot without changing the regions in which the vertices of the maximum square are located. The shift causes the size of the side length of the square to change. Also, it may change the (left or right) side in which the smaller square occurs. The smaller square is used to determine the SNM.

Next, we calculate SNM using the analytical I - V equations in the three regions of interest.

3.1 Calculation of VL-VR in region 1

Before applying KCL at node R , we use some approximations. For NR , since V_{gs} is less than V_{thln} , V_{dsat} is very small, and hence, we may write

$$1 + \frac{V_{dsatNR}}{E_{sat}L} \approx 1 \quad (21)$$

The voltage of VR is also close to V_{dd} making V_{ds} of PR very small, and hence, we have

$$1 + \frac{V_{dsPR}}{E_{sat}L} \approx 1 \quad (22)$$

With these approximations, using Eqs. (1) and (13), the current equations for these transistors may be written as

$$\begin{aligned} I_{dsPR} = & K_{PR} [a_{2PR}(V_{dd} - VL - b_{2PR})^2 + c_{2PR} \\ & - \frac{1}{2}(V_{dd} - VR)](V_{dd} - VR) \end{aligned} \quad (23)$$

$$\begin{aligned} I_{dsNR} = & K_{NR} a_{1NR} (VL - b_{1NR})^2 \times \\ & [(\frac{1}{2}V_{As1NR}a_{1NR} - a_{1NR})(VL - b_{1NR})^2 + VR]/V_{As1NR} \end{aligned} \quad (24)$$

Since AR is off in this region, we have

$$I_{dsNR} = I_{dsPR} \quad (25)$$

In Eq. (24) as VR is near V_{dd} and VL is small and close to b_{1NR} , $VL - b_{1NR}$, is small. Thus, I_{dsNR} may be approximated as

$$I_{dsNR} = K_{NR} a_{1NR} (VL - b_{1NR})^2 \times VR / V_{As1NR} \quad (26)$$

From Eqs. (23)-(26), we can find VR as a function of VL as

$$VR = f(VL) \quad (27)$$

After solving the equations and finding the analytical expression for $f(VL)$, we see that $(VL - b_{1NR})^2$ is the dominant term and hence we may approximate the function by

$$f(VL) \approx V_{dd} - m(VL - b_{1NR})^2 \quad (28)$$

where m can be found from the above equation by taking its second derivative with respect to VL and evaluating it at any point in region 1. For simplicity, we choose the point of $VL = b_{1NR}$, and therefore, obtain

$$\begin{aligned}
m &= -\frac{1}{2} \frac{\partial^2 f(VL)}{\partial VL^2} \Big|_{VL=b_{1NR}} \\
&= \frac{K_{NR} \times a_{1NR}}{K_{PR} \times V_{As1NR} [a_{2PR}(V_{dd} - b_{1NR} - b_{2PR})^2 + c_{2PR}]} \quad (29)
\end{aligned}$$

3.2 Calculation of VL-VR in two last regions

To obtain VL - VR in regions 3 and 4, we need a simple equation for the current of AR in the saturation region. Considering that $V_{ds}=V_{gs}$ for AR , we can rewrite the drain current of AR as

$$I_{dsAR} = \frac{1}{2} k_{AR} \times E_{sat} L \times \frac{Z_1}{Z_2^2} \times Z_3 \quad (30)$$

where

$$Z_1 = \frac{[a_{2AR}(V_{gsAR} - b_{2AR})^2 + c_{2AR}]}{V_{As2AR}V_{gsAR} + V_{AhAR}} \quad (31)$$

$$Z_2 = E_{sat} L + a_{2AR}(V_{gsAR} - b_{2AR})^2 + c_{2AR} \quad (32)$$

$$\begin{aligned}
Z_3 &= [(V_{As2AR} + 1)V_{gsAR} + V_{AhAR}] Z_2 \\
&- E_{sat} L(a_{2AR}(V_{gsAR} - b_{2AR})^2 + c_{2AR})
\end{aligned} \quad (33)$$

Note that the variation of Z_1 by V_{gsAR} is negligible, and hence, for our calculations we use its value at $V_{gsAR} = b_{2AR}$ which is

$$Z_1 = \frac{c_{2AR}^2}{V_{As2AR}b_{2AR} + V_{AhAR}} \quad (34)$$

Z_2 is also approximately constant for V_{gsAR} between V_{thl} and b_{2AR} and increases slightly by increasing V_{gsAR} for $V_{gsAR} > V_{thl}$. We can also assume Z_2^2 constant but to increase the accuracy, we may use a geometric average by using the values of Z_2 evaluated at two boundary V_{gs} values as,

$$\begin{aligned}
Z_2^2 &\approx Z_2 \Big|_{V_{gsAR}=b_{2AR}} \times Z_2 \Big|_{V_{gsAR}=V_{thl}} \\
&= (E_{sat} L + c_{2AR})(E_{sat} L + a_{2AR}(V_{thl} - b_{2AR})^2 + c_{2AR}) \quad (35)
\end{aligned}$$

The simulations also show that I_{dsAR} has a linear relationship with V_{gsAR} . By substituting the approximate values of Z_1 and Z_2^2 , into Eq. (30) and taking the derivative with respect to V_{gsAR} at a point like b_2 , it is possible to obtain the slope of I_{dsAR} with respect to V_{gsAR} , denoted by s_{AR} , as

$$\begin{aligned}
s_{AR} &= \frac{\partial I_{dsAR}}{\partial V_{gsAR}} \Big|_{V_{gsAR}=b_{2AR}} = \frac{1}{2} K_{AR} E_{sat} L \\
&\times c_{2AR}^2 (1 + V_{As2AR}) \times (V_{As2AR}b_{2AR} + V_{AhAR})^{-1} \\
&\times (E_{sat} L + a_{2AR}(V_{thl} - b_{2AR})^2 + c_{2AR})^{-1} \quad (36)
\end{aligned}$$

Substituting V_{gs} by V_{thl} in Eq. (10) and noting that V_{thl0} is the threshold voltage for V_{gs} equal to V_{thl}

$$a_2(V_{thl} - b_2)^2 + c_2 = V_{thl} - V_{thl0} \quad (37)$$

As discussed before, the right hand side is very small and approaches zero as the channel length increases. Therefore, we can approximate s_{AR} as

$$s_{AR} = \frac{1}{2} K_{AR} \times \frac{c_{2AR}^2 (1 + V_{As2AR})}{(V_{As2AR}b_{2AR} + V_{AhAR})} \quad (38)$$

The simulations show that for the three technologies

$$b_2 + \frac{V_{Ah}}{V_{As2}} \approx 1 \quad (39)$$

Thus,

$$s_{AR} = \frac{1}{2} K_{AR} \times c_{2AR}^2 \times \left(1 + \frac{1}{V_{As2AR}}\right) \quad (40)$$

Since Z_1 and Z_2 are almost constant and I_{dsAR} has a linear relationship with V_{gs} , it may be concluded that Z_3 should have a linear dependence on V_{gs} . To find this linear relation, we rewrite Eq. (33) as

$$Z_3 = (V_{As2AR} + 1)Z_2 \times \left(V_{gsAR} + \frac{\frac{E_{sat}L(Z_2 - E_{sat}L)}{Z_2}}{V_{As2AR} + 1} \right) \quad (41)$$

Using the value of Z_2 evaluated at $V_{gsAR} = b_{2AR}$ yields

$$Z_3 = (V_{As2AR} + 1)Z_2 \times \left(V_{gsAR} + \frac{\frac{E_{sat}Lc_{2AR}}{E_{sat}L + c_{2AR}}}{V_{As2AR} + 1} \right) \quad (42)$$

The value of I_{dsAR} at $V_{gsAR} = 0$, denoted by h_{AR} , is obtained from

$$h_{AR} = s_{AR} \frac{\frac{E_{sat}Lc_{2AR}}{E_{sat}L + c_{2AR}}}{V_{As2AR} + 1} \quad (43)$$

Finally I_{dsAR} versus V_{gsAR} can be estimated as a linear function given by

$$I_{dsAR} = s_{AR} \times V_{gsAR} + h_{AR} \quad (44)$$

In region 3, PR is in the saturation region with V_{sg} less than $|V_{thlp}|$ and is *off* in region 4. In these two regions, the AR and NR currents are large while the PR current is small and can be ignored for the sake of simplicity. Here, as discussed in the beginning of this section, it is better to find VL versus VR for the read SNM calculation.

$$I_{ds-AR} = I_{ds-NR} \quad (45)$$

$$\begin{aligned} & K_{AR} E_{sat} L VR (a_{2NR} (VL - b_{2NR})^2 + c_{2NR}) \\ &= (\frac{1}{2} K_{AR} E_{sat} L - a_{2AR}) VR^2 \\ &+ (s_{AR} V_{dd} + h_{AR} - E_{sat} L s_{AR}) VR \\ &+ E_{sat} L (s_{AR} V_{dd} + h_{AR}) \end{aligned} \quad (46)$$

From the above equations, VL may be found. To simplify this equation, we note that for high V_{gs} , V_{gseff} has a linear relationship with V_{gs} as shown in Fig. 5, so $V_{gseffNR} = a_{2NR} (VL - b_{2NR})^2 + c_{2NR}$ can be approximated by a linearity relation as

$$V_{gseffNR} = \alpha VL + \beta \quad (47)$$

where α and β may be found from evaluating the function at any point denoted by VL_m in these regions (regions 3 and 4)

$$\alpha = 2a_{2NR} (VL_m - b_{2NR}) \quad (48)$$

$$\beta = a_{2NR} [b_{2NR}^2 - VL_m^2] + c_{2NR} \quad (49)$$

The best point to minimize the approximation error for VL_m is the beginning of region 3. For obtaining VL_m , noting VR is small (and hence, $1 + VR/E_{sat}L \approx 1$), we may rewrite Eq. (45) as

$$(VR - V_{gseffNR} - \frac{S_{AR}}{K_{NR}})^2 = U \quad (50)$$

where

$$U = (V_{gseffNR} + \frac{S_{AR}}{K_{NR}})^2 - \frac{2}{K_{NR}}(S_{AR}V_{dd} + h_{AR}) \quad (51)$$

Taking the second derivative of Eq. (50) with respect to VL , we obtain

$$2[VR' - 2a_{2NR}(VL - b_{2NR})]^2 + (VR'' - 2a_{2NR})(VR - V_{gseffNR} - \frac{S_{AR}}{K_{NR}}) = U'' \quad (52)$$

Here, we need the expression for VR as a function of VL . At the beginning of region 3, NR is at the boundary of linear and saturation, and hence, V_{dsNR} is equal to V_{dsatNR} .

$$V_{dsNR} = V_{dsatNR} = V_{gseffNR} \quad (53)$$

Using the approximate equation for V_{dsatNR} , it is possible to write

$$VR = a_{2NR}(VL - b_{2NR})^2 + c_{2NR} \quad (54)$$

Taking the first and second derivative of Eq. (54) with respect to VL , we obtain, respectively,

$$VR' = 2a_{2NR}(VL - b_{2NR}) \quad (55)$$

$$VR'' = 2a_{2NR} \quad (56)$$

Substituting Eqs. (55) and (56) in Eq. (52) yields

$$U'' = 0 \quad (57)$$

Thus, VL_m is obtained easily as

$$VL_m = b_{2NR} + \sqrt{-\frac{(m_{AR} + K_{NR}c_{2NR})}{3K_{NR}a_{2NR}}} \quad (58)$$

Having found VL_m , α and β can be found from Eqs. (48) and (49), respectively. Finally, substituting $V_{gseffNR}$ from Eq. (47) into Eq. (46), VL versus VR can be easily achieved. Finally, note that VL_m could have been obtained by solving Eqs. (50) and (54). Since solving these equations was very difficult, we took the approach explained here.

3.3 Read SNM calculation

In Fig. 13, the butterfly curves of HSPICE simulations and the proposed technique are compared. As is evident from the figure, the error is very small. The VL - VR relations obtained in the three regions are simple and hence may be used for the read SNM calculation. As shown in Fig. 13, for calculating SNM we can intersect the normal curve and the mirrored one by the line of $VR = VL + a$ (Bhavanagarwala *et al.*, 2001).

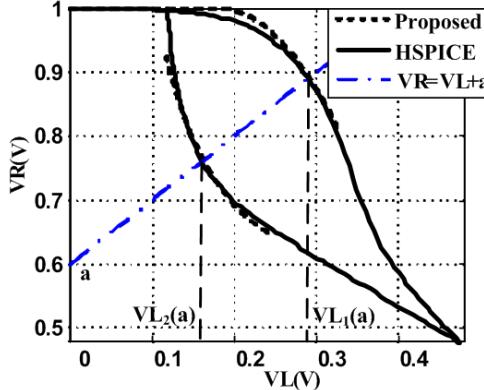


Fig. 13 Butterfly curve in the read mode for calculating read SNM

- 1: Obtain m from (29)
- 2: Obtain $VR=f(VL)$ in region 1 from (28) and (29)
- 3: Obtain VL_1 by intersecting $VR=VL+a$ by the above equation
- 4: Obtain VL_m from (58)
- 5: Obtain α and β from (48) and (49), respectively
- 6: Obtain $V_{\text{reset}/VR}$ from (47) and inserting into (46)
- 7: Obtain $VL=f(VR)$ from (46)
- 8: Replace the parameters of the left transistors by those of the right transistors and do mirroring to find $VR=g(VL)$ in regions 3 and 4
- 9: Obtain VL_2 by intersecting $VR=VL+a$ by the above equation
- 10: Obtain a by setting to zero the differential of VL_1-VL_2 with respect to a
- 11: Obtain SNM from (59) and (60)

Fig. 14 SNM calculation steps

Note that to obtain the mirrored curve in region 1, we could use the formulas in regions 3 and 4 but we should replace the parameters of the left transistors of AL and NL by those of the right transistors of AR and PR and do mirroring. For each a , this line intersects the normal and mirrored curves at two points, denoted by (VL_1, VR_1) and (VL_2, VR_2) . The points are determined by equating the equation of this line by the equations of the butterfly curves. The SNM may be found from the maximum separation of the points or side length of the square encompassing in the butterfly curves as

$$SNM = \max(\text{side length}) \quad (59)$$

where

$$\text{Side length} = VL_1(a) - VL_2(a) \quad (60)$$

Using the expressions obtained in the previous section, an analytical relation for the SNM (*side length*) is obtained. Fig. 14 illustrates the steps that should be taken for the SNM calculation.

4 Results and Discussion

In this section, we discuss the results of the analytical SNM model for different technologies. The results also include the study of the effects of process variations, NBTI, and the minimum supply voltage required for a target yield in the presence of the process variations. In Fig. 15, the read SNMs calculated using the proposed model and the HSPICE simulations as a function of the β -ratio (the relative strength of the pull down transistors to access transistors) are compared. The results are presented for three CMOS technologies of 32, 45, 65, and 90 nm. As shown in this figure, our read SNM model has very high accuracy. The maximum errors were 1.5, 1.7, 1.4, and 1.5% for the 32, 45, 65 and 90 nm technologies, respectively. The errors are much less than those reported in the recently published work for the 70 nm technology (maximum 8%) (Chen *et al.*, 2007). In the case of the work presented in (Bhavanagarwala *et al.*, 2001), the maximum error of the model was more than 3% for a 0.18 μm process. In addition, the model in (Bhavanagarwala *et al.*, 2001) suffers from complexity and relies

on fixed point iteration to reach self-consistency. This shows higher accuracy for the SNM model presented in this work as compared to existing models. The high level of accuracy makes the model appropriate for practical designs. In fact, using the flowcharts given in Figs. 9 and 14, we can calculate the SNM much faster than with HSPICE without requiring the type of numerical calculations performed in HSPICE simulations.

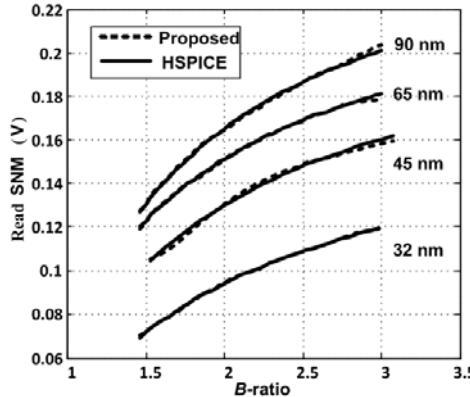


Fig. 15 Read SNM curves with respect to β -ratio for 32, 45, 65, and 90nm technologies

Next, we study the accuracy of the model in the presence of process variations and negative bias temperature instability (NBTI) effect. For this study in which we consider threshold voltage variations, a Gaussian distribution for the threshold voltage is assumed (Agarwal and Nassif, 2008). It should be noted that random dopant fluctuation (RDF) usually dominates the total threshold voltage variation (Orshansky *et al.*, 2008). The value of the standard deviation for this distribution, denoted by $\sigma V_{th,RDF}$, is given by (Li *et al.*, 2009)

$$\sigma V_{th,RDF} = 3.19 \times 10^{-8} \frac{t_{ox} N_A^{0.401}}{\sqrt{WL}} \quad (61)$$

where t_{ox} is the oxide thickness and N_A is the doping density. For the 32nm technology, the 3σ value (for the minimum size transistor) becomes slightly more than 10% of nominal threshold voltage. Other sources of variations may increase this value. To consider the worst case condition, we considered $3\sigma = 20\%$ of the nominal value. The variations, which are mainly induced by random dopant fluctuation (RDF), are highly uncorrelated (independent) (Agarwal and Nassif, 2008).

The values obtained from the distributions were applied to V_{thl} of transistors in the proposed model and V_{th0} in the HSPICE simulations. The other fitting parameters were assumed to be constant. Also, we considered the NBTI effect which is responsible for the threshold voltage increase of PMOS transistors over time when a negative bias is applied (Schroder and Babcock, 2003). Previous works have shown that the read SNM was degraded by the NBTI effect (Kang, 2007). Fig. 16 shows the PDF of the read SNM calculated by the HSPICE simulations and our proposed model under process variations and NBTI in the 32nm technology. The results which were obtained after 10,000 Monte Carlo simulations showed that our models (SNM and $I-V$) had high accuracy in the presence of both process variation and NBTI (aging effect) while it is evaluated in a very short period of time due to its analytical nature. The computer runtime was 0.23s and 48,949 s when our analytical model and HSPICE simulations, respectively, were used the study of the SNM variation in the presence of process variations. The high accuracy of the model makes it a much more efficient technique for calculating the read SNM than HSPICE simulations when we study the impact of process variations and NBTI on the read SNM of the SRAM cell. It should be mentioned that both the transistor width (W) and length (L) also will have variations in the presence of the process variations. These variations are highly correlated giving rise to small impacts on stability metrics such as read SNM (Mukhopadhyay, 2005), and hence, are ignored in this study.

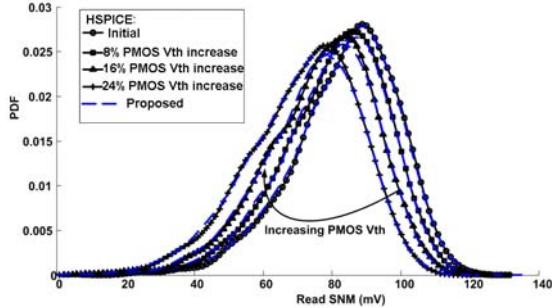


Fig. 16 Probability distribution function (PDF) of read SNM calculated by the HSPICE simulations and our proposed model under process variations and NBTI effect with 8, 16, and 24% increase in PMOS threshold voltage in 32 nm technology

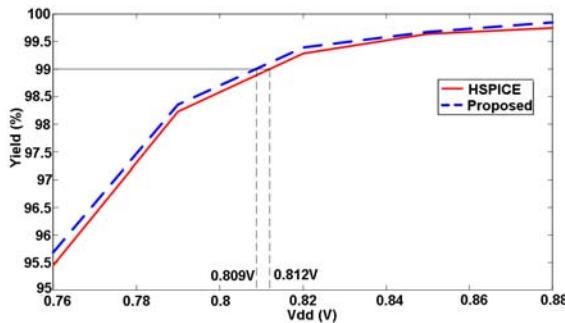


Fig. 17 Yield versus supply voltage for the 32nm technology. A target read SNM of 27 mV was assumed

One of the applications of the read SNM model is to obtain the minimum supply voltage that satisfies the target yield (for example 99%) (Park *et al.*, 2010). The voltage is denoted by V_{ddmin} . In a low power design, the supply voltage should be minimized as much as possible. On the other hand, the reduction of the supply voltage may cause deterioration in the yield (Park *et al.*, 2010). We investigated the effect of V_{dd} scaling on the yield in the presence of process variations in the 32 nm technology. The results of this study performed using both the model and HSPICE simulations are shown in Fig. 17. Since for higher V_{dd} s, failure events rarely occur, 50,000 Monte Carlo simulations were needed for the yield calculation. The figure which plots the SNM yield versus the supply voltage again shows very good accuracy for the model. A target read SNM of 27 mV was assumed for this study. For a target yield of 99%, V_{ddmin} of 0.809 V and 0.812 V are predicted by the model and simulation, respectively.

5 Conclusions

In this work, an accurate model for I - V characteristics of sub-90-nm MOSFET in the linear and saturation regions were proposed. Contrary to the n^{th} -power law, in our proposed model, the current relations with the voltages had integer powers making it suitable for hand calculations and analysis. The accuracy of the model was verified for the 90, 65, 45, and 32 nm CMOS technologies. The model showed better accuracy than the n^{th} -power and BSIM3v3 models. The procedure for extracting the model parameters was also described. Next, the read SNM was calculated using the proposed I - V model. We used the criteria of the side length of the maximum square encompassed in the butterfly curves as the SNM. To obtain the read SNM, the voltage transfer characteristic was approximated in the regions where the vertices of the square were laid. The read SNM obtained from the approach had a maximum error of approximately 1.7% for the three technologies. The accuracy of the model also was verified in the presence of process variations and negative bias temperature instability (NBTI) effect. Moreover, it was shown that the model could accurately predict the minimum supply voltage

required for a target yield. It should be noted that the analytical model for the I - V characteristic of highly scaled transistors is expected to have wide applications to many other circuit analysis and optimization problems thanks to the integer power relation between current and voltage.

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