

Introductory Invited Paper

Workload and temperature dependent evaluation of BTI-induced lifetime degradation in digital circuits



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ABSTRACT

In this work, we investigate the co-dependency of die temperature and bias temperature instability (BTI) and their combined effect on the lifetime of VLSI circuits. The investigation considers the impact of die temperature in increasing the effect of the BTI as well as changes in the die temperature due to the BTI-induced threshold voltage alterations. In addition, the impact of workloads on the degree of the BTI-induced degradation in VLSI circuits is studied. This impact accounts for the direct influence of the signal probability of the internal nodes under the given workload as well as its indirect influence due to power consumption and temperature changes of the circuits. The study is performed by using a simulation framework that captures dynamic changes in the operating temperature and application workload. Simultaneous consideration of the dynamic workload and operating temperature enables one to accurately predict the circuit lifetime. To assess the accuracy of the proposed approach, the estimated delay degradations caused by the Negative BTI (NBTI) for some large circuits from ISCAS'89 and ITC'99 benchmark suites when circuits are simulated under dynamic (both temperature and workload are updated periodically), semi-static (either temperature or workload is updated periodically), and static (no updating is performed) scenarios are compared. Simulation results obtained in a 45 nm CMOS technology, reveal that the predicted timing degradation in the case of the dynamic scenario is significantly different than those of the other scenarios. The differences ranged from –135% to +98% for the considered circuits in this work. The large differences demonstrate that for accurate estimation of the circuit lifetime under the BTI effect, the dynamic scenario should be adopted as part of the standard design flows.

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1. Introduction

The reliability of electronic products, which is known as the distinction of the electronics industry, has been made to improve steadily over the years [1]. In recent years, due to complexities which exist in the state-of-the-art technologies, considerably more efforts are needed to keep the long established trend. Examples of the complexities which are due to the technology scaling include Bias Temperature Instability effects (BTI), Time Dependent Dielectric Breakdown (TDDB), and Hot Carrier Injection (HCI) which may threaten the correct functionality of the circuit over

its lifetime. This would lead to a significant reduction of the system reliability. Among the aforementioned phenomena, the BTI effect is considered as a dominant reliability concern as the gate oxide becomes thinner in highly scaled technologies [2]. This BTI phenomenon causes the increase in the absolute values of the threshold voltage of the transistors over the time degrading the circuit speed and decrease in the subthreshold leakage for a given supply voltage. The former may reduce the lifetime of the circuit which has a specified speed requirement [3] while the latter reduces the static power. The level of the NBTI degradation depends on the nitrogen (N) distribution profile induced in the gate insulator during the fabrication process. The impact of the BTI phenomenon depends on the amount of stress voltage (V_{stress}), operating temperature, and the physical parameters of the device such as the gate oxide thickness and inversion layer carrier density [4,5]. In addition, the impact is a strong function of the duty cycle of the applied signal (stress).

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To describe the phenomenon more, note that the BTI effect consists of two different phases which are called stress and recovery phases. In the stress phase, in the case of PMOS transistors, when the devices are ON which causes the gate oxide field (E_{ox}) increasing the generation of interface traps by the amount of ΔN_{IT} and hole trapping phenomenon in the bulk traps. This results in the increase in the magnitude of threshold voltage of the PMOS devices. On the other hand, the threshold voltage degradation caused by the positive BTI (PBTI) in NMOS transistors, is generally perceived to be due to electron trapping (ΔN_{ET}) in the High-K (HK) bulk insulator traps [6]. In the recovery phase, where the gate oxide field is removed, the magnitude of the threshold voltage decreases toward its initial value due to the fact that some of trapped electrons and holes are annihilated in the cases of PBTI and NBTI, respectively. Because of the rapid retrieval at the beginning stage of the recovery phase, even in a small recovery period, greatly reduces the overall degradation [3]. However, since not all of the trapped charges are retrieved, the consequent stress and recovery phases result in a net $|V_{th}|$ increase.

The degradation magnitude is a strong function of time (through a power-law time-dependence), operating temperature, the amount of the negative bias, and the duty cycle of the applied signal to the gate of the PMOS transistor [4,5]. The change of the threshold voltage due to the BTI phenomenon can be modeled as [7]

$$|\Delta V_{th}(t)| \approx A \cdot SP^n \cdot t^n \quad (1)$$

where A is a technology dependent factor and is a function of different parameters such as die temperature, supply voltage, and initial threshold voltage of transistor, SP is the duty cycle or signal probability of the applied signal to the gate of the transistor, and t is the elapsed lifetime. Also, n is typically assumed between 0.16 and 0.25 (0.1 and 0.2) for NBTI-induced (PBTI-induced) degradation [3,8]. Note that both NBTI and PBTI are temperature-activated processes. The effect of the temperature dependence is included in A through an exponential relationship [3,9,8]. In other words,

$$A \propto \exp\left(\frac{-E_a}{K_B T}\right) \quad (2)$$

where E_a is the activation energy, K_B is the Boltzmann's constant, and T is the temperature. As a result, the threshold voltage change becomes proportional to the temperature. The strong dependence implies that a small increase in the operating temperature may cause a large threshold voltage change. It should be noted that the power consumption varies over time, it can dynamically alter the operating temperature, T , in Eq. (2). In addition, since the workload may strongly affect the (dynamic) power consumption, the die temperature can considerably vary with the workload variation too. Hence, the power consumption as well as the workload variation should be considered for a more accurate lifetime prediction of the circuit. Also, one should note that as mentioned before, the increase in the threshold voltage absolute value (caused by the BTI effect), decreases the static power through an exponential relation. The impact of this decrease on the operating temperature also should be considered in the lifetime prediction.

In addition to the effect of the workload on the die temperature variations due to the power consumption changes, the workload changes the duty cycle of the applied stress to the transistors [6,5]. The reason is that the operating conditions (including the voltage and frequency) and the inputs of different parts of the circuit are changed based on the workload. This causes different delay degradations owing to asymmetric (non-uniform) stress and temperature distributions for various parts of the circuit. The works based on the conventional reliability analysis have assumed either a DC stress condition or an average duty cycle when considering an

AC stress condition. Since during the actual operation, different parts of the circuit may have different operating modes (such as standby mode where the clock gating may be invoked), even using an average duty cycle for considering the AC stress condition may not predict the impact of the BTI effects with a sufficient accuracy [3,10]. Thus, for more accurate aging analysis and lifetime prediction, considering application workload is inevitable.

In this work, we investigate the importance of considering both the die temperature and workload variation on aging analysis and lifetime prediction in the presence of the BTI phenomenon. Although in this work, we only focus on the NBTI, the approach may be easily used for high- κ gate dielectrics metal gate transistors by including the degradation model due to the PBTI effect. The investigation is performed using a simulation framework which considers dynamic variations of the operating temperature, workload, and signal probability of the internal nodes. The rest of the paper is organized as follows. In Section 2, the related works are briefly reviewed while the problem statement is presented in Section 3. The simulation framework is described in Section 4 and the results are discussed in Section 5. Finally, Section 6 concludes the paper.

2. Related works

The NBTI-induced effects have been extensively studied in recent years. These works include presenting techniques for lifetime prediction, NBTI-aware timing analysis, and reliability improvement of VLSI circuits such as memories and processors in the presence of NBTI. In this section, owing to the focus of this work, on the lifetime prediction, we only review some related works presented for NBTI-aware lifetime prediction. A predictive modeling of the NBTI effect, which was presented in [10] and further developed in [3], proposed an upper bound for the NBTI delay degradation under the time varying (AC) stress. The delay models were utilized for the aging analysis of combinational circuits as a function of the slew rate and load capacitance. The models, however, were complicated as they used the Taylor series expansion and Chebyshev polynomial to fit the gate delay degradation. The works presented in [11] and [12], used the upper bound of the NBTI delay degradation, given in [3], to predict the timing violations of the combinational logic path under the NBTI-induced asymmetric aging. In [11], the aging-induced gate delay degradation for the library cells was formulated as a function of the threshold and supply voltages. The expression then was used to calculate the degradation as a function of the threshold voltage shift without relying on the time consuming circuit simulations. In [13], some aging models for estimating the delays of digital gates were proposed. These models were used to estimate the delay shifts in the critical paths of the circuit. In all of the above works, the operating temperature and workload were assumed to be constant. For example, in the cases of [7] and [9], the AC stress condition with constant average duty cycle was supposed. Some earlier works (see, e.g., [14]) considered a DC stress condition. As was discussed before, during the actual circuit operation, different parts of the circuit may have different modes, and hence, the average AC stress condition may not enable us to accurately predict the impact of the NBTI effect on the lifetime [3,15].

Some recent works have included the workload dependency in the lifetime prediction in the presence of the NBTI effect. In [16] and [17], while running real world applications, the aging effects at different hierarchical design levels of an embedded processor have been analyzed. The results presented in [16] and [17] for different application workloads reveal that the timing degradation at a given time can vary from 2% to 11%. As mentioned before, different workload conditions in different periods of the circuit lifetime

may lead to unequal aging rates for different parts of the circuit. The asymmetric aging due to the workload dependency would show themselves more clearly when power management techniques such as clock gating schemes are invoked [11,18,19]. This has been the motivation for proposing some aging mitigation technique for reducing the effect of the asymmetric aging on circuit timing by simultaneous consideration of NBTI-induced degradation on clock tree and logic path [15]. In all of the aforementioned works which considered the workload variations in the lifetime predictions, the operating temperature was assumed to be fixed.

There are some works which have considered the temperature variation during the lifetime predictions [7,20,21]. In [7], an analytical approach was presented to predict the probability density function and covariance of the temperatures and voltage droops of a die in the presence of the BTI and process variation. The approach consisted of multiple statistical nested loops iteratively executed until the mean and sigma of the considered lognormal distributions for the leakage power, temperature, and BTI effect converge. The approach, however, only considered the mutual effect of BTI and the leakage power without considering other components of power consumption such as short circuit and dynamic (charging/discharging) power. The approach made use of analytical expressions for modeling the impacts of both the BTI phenomena and process variations simultaneously. This makes the approach intricate prohibiting the inclusion of the circuit topology, transistor sizing, and the different aging rates of the cascaded stages. As will be discussed later, these parameters strongly influence the impact of BTI effect on the overall performance of the circuit. In addition, the lognormal distributions were considered for all profiles of leakage, thermal, voltage droops, and BTI effect which may not be accurate. Finally, to reduce the computational time required for the analysis, the expected lifetime is divided to many time intervals where complex nested loops should be executed. This increases the computational resources required for performing the analysis.

In [20], an estimation method for the temporal performance degradation of digital circuits based on a PMOS threshold voltage degradation model was proposed. To consider the effect of the temperature on the lifetime prediction, the circuit was assumed to work at the temperature of T_{High} when the circuit was in the active mode and at the temperature of T_{Low} when the circuit was in the standby mode. Then, the NBTI-induced degradation model was modified by replacing the time with an equivalent stress time which was calculated as a function of the diffusion coefficients ratio in the high and low operation temperatures. While the work presented in [20] did not assume a fixed temperature, it only considered two fixed operating temperatures which may not resemble the actual operating conditions where the temperature varies dynamically based on workload. In [21], a simulation framework which dynamically estimated the effect of NBTI on power consumption of the circuit, and hence, the operating temperature was proposed. In the work, the static power was assumed to be on average 50% of the total power. Based on this assumption, over the time the increase in the threshold voltage decreased the static power which in turn reduced the chip temperature. The decrease in the temperature lowered the rate of the aging which is a strong function of the temperature. The work only considered the effect of the NBTI induced threshold voltage (V_{th}) change on the static power without considering the effect on the total power including dynamic power.

In this work, the interwoven effects of both dynamic workload and temperature on the NBTI induced circuit lifetime degradation are investigated using a simulation framework for the circuit lifetime prediction which considers dynamic workload and operating temperature variations. Since the focus of this work is on showing the importance of considering both dynamic workload and temperature simultaneously in improving the accuracy of the BTI

induced circuit lifetime degradation, the impact of the process variation on the circuit performance is not included in this investigation. In the next section, we describe the problem statement.

3. Problem statement

As mentioned before, the BTI phenomena alter the circuit characteristics over the time and hence, determine the aging and reliability of the circuit. These phenomena depend on the operating temperature and duty cycle of the circuit nodes which change dynamically making the prediction of the reliability and the circuit lifetime a challenging task. In addition, the prediction becomes further complicated by considering the mutual effects of the workload (which affects the duty cycle) and temperature. In this section, we will describe the relationships between temperature, workload and NBTI-induced aging rate.

When considering the workload, one should note that there are different modes of operation. More specifically, for the circuit which is not used for a long time, the applied signals are unchanged. If no BTI reduction technique is used, the signals may be such that the BTI effect is enhanced (static stress) increasing the aging rate of the circuit or vice versa. If the circuit is active, the activity profile of the internal nodes of the circuit defines the duration and the amount of the stress condition applied to the different parts of the circuit. For this case, the chance of changes in the applied signals is high, lowering the aging rate thanks to the smaller duty cycle amounts. The active circuit normally has a higher operating temperature leading to higher aging rates. These facts stress out the importance of considering the workload during the lifetime prediction of the circuit in the presence of the BTI phenomena. In fact, considering application workloads can substantially changes product reliability predictions [17].

On the other hand, the workload affects the operating temperature which strongly influences the impact of the NBTI. The circuit temperature is a strong function of the power consumption modeled by [9]

$$T = T_a + P \times R_{thermal} \quad (3)$$

where T_a is the ambient temperature, P is the total power including both dynamic and static power and $R_{thermal}$ is the equivalent thermal resistance of the circuit.

The total power is the sum of the charging/discharging power of the node capacitance, power due to the short-circuit currents, and the static power. The last component which is mainly due to the subthreshold current in the static CMOS circuits, could form a major portion of the power consumption especially when the circuit activity is low. Due to the exponential dependence of the subthreshold current on the temperature, the increase in the power consumption causes a significant increase in the static power which further enlarges the temperature following a positive feedback behavior. On the other hand, the temperature increase exacerbates the effect of the NBTI phenomenon in increasing the threshold voltage. This reduces the subthreshold current moving in the opposite direction of increasing the static power. The net effect (increase or decrease of the leakage) depends on the workload profile and the amount of temperature change.

The charging/discharging power of the node capacitance and power due to the short-circuit currents form the dynamic power. For the case of charging/discharging power, the node capacitance consists of interconnect capacitance (which is small for local interconnects and independent of voltage), and next gate input capacitance, and gate self-loading capacitance, which the latter two are voltage dependent. Since the threshold voltage of the transistors affect the rise/fall times of the nodes, the BTI effect influences the time-variation profile of these capacitances (and hence, the

dynamic power) over time. Similarly, in the case of the short circuit power, the rise/fall times determine the profile of the short circuit current based on the threshold voltages, circuit topology, and workload.

All of the above discussions emphasize the fact that one may not predict the power change trend with the NBTI accurately for large circuits without considering the time-dependent variation of temperature and workload. Based on this discussion, the trend of the total power consumption may not be predicted a priori, and hence, it should be determined using circuit simulations for the application workload. Next, to further elaborate on the above discussion, we demonstrate the variations of temperature and power (due to the variation of the workload) for some circuits.

First, the thermal profiles of the b21 and the s38584 circuits from the ITC'99 and ISCAS'89 benchmark suites under four different workloads (see Section 4 for more details about the workloads) of high load, medium load, low load, and near idle has been plotted in Figs. 1 and 2 respectively. The thermal profiles are extracted using Thermal Analysis tool of the Cadence Encounter Power System (EPS). After synthesizing the circuit, Power Analysis tool, which works based on the activity profile of the input and internal nodes, is invoked. Finally, based on the power report, the thermal analysis tool generates the thermal report/profile of the circuit. As is apparent from these figures, there are considerable temperature differences for the same point on the circuit for these workloads yielding the temperature differences up to 25 °C and 17 °C in b21 and s38584 respectively. For other benchmarks, the maximum values are 11 °C, 21 °C, 22 °C, 9 °C, and 15 °C for b15, 17, b20, s35932 and s38417 circuits respectively. This amount of the temperature differences can significantly affect the degradation rate caused by the BTI effects. In Fig. 3, we have drawn the

histograms of the duty cycles (the probability of the internal node signal to be zero) of internal nodes of, e.g., the circuit s38714 from ISCAS'89 benchmark suite for those workloads. The results were obtained by running the simulator for the circuit for a 10 year period of time. As is evident from these figures, the duty cycle which considerably affects the aging rate is a strong function of the workload. The maximums of the histograms occur at [30%, 35%] for the high load workload and [0%, 5%] the other workloads.

Next, the distributions of the maximum and average changes of the internal and static powers with the reference to the corresponding time zero values for the circuit b21 are drawn in Figs 4 and 5, respectively (see Section 4 for more details about power calculation method). The internal power included both the short circuit and capacitance charging/discharging of the cells. The results were obtained for ten years of the circuit operation. As the results reveal, the change in the average of the internal (static) power ranges from the interval [−80%, −70%] ([−100%, −90%]) to [190%, 200%] ([60%, 70%]) while the maximum occurs in the [−20%, −10%] ([−30%, −40%]) interval. It should be noted that the impacts of the aging which affect both the internal and static powers have been considered in obtaining the results in these figures.

Finally, in Fig. 6 a time window of the internal power of four cascaded NAND2X1 gates inside b21 circuit is plotted. Since these gates have been placed close to each other in the layout of the circuit, they have about the same temperature changes. The differences between the time-dependent characteristics of the internal power somehow show that, the trend of aging could be different even for the same gates. This is attributed to the fact that the activity profiles of the input nodes of these gates are different causing different internal powers. In addition, internal power depends on

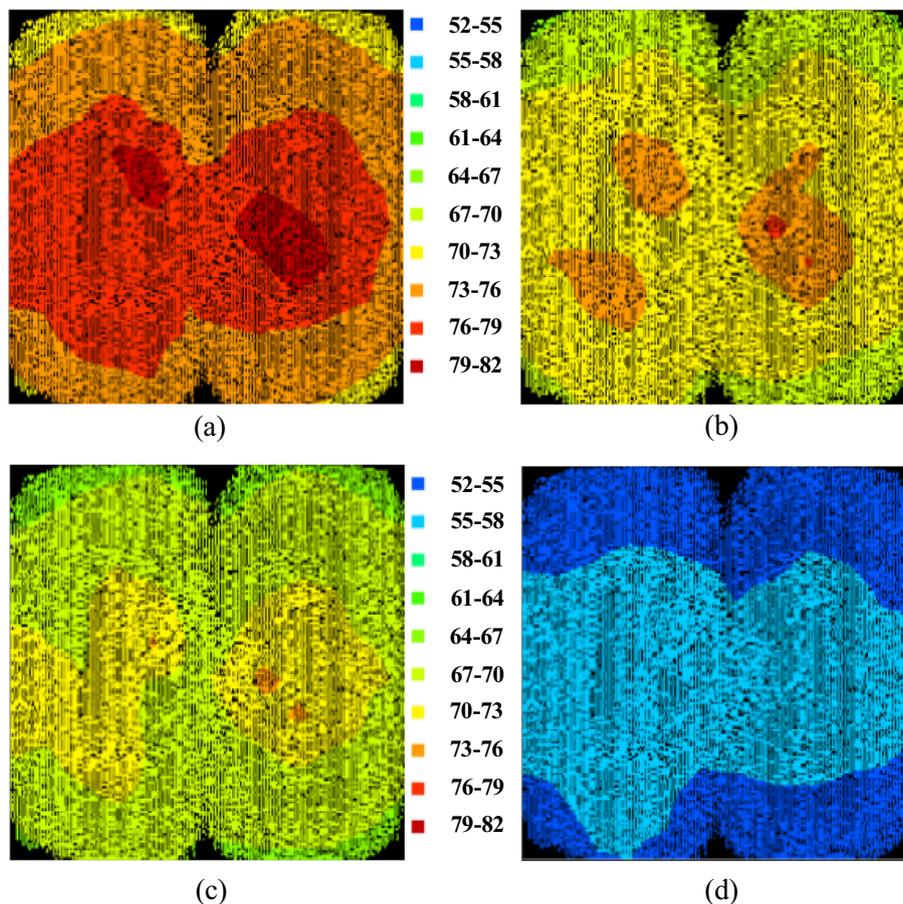


Fig. 1. Temperature profiles (°C) for the b21 benchmark circuit under four different workloads of (a) high profile, (b) medium profile, (c) low profile, and (d) near idle.

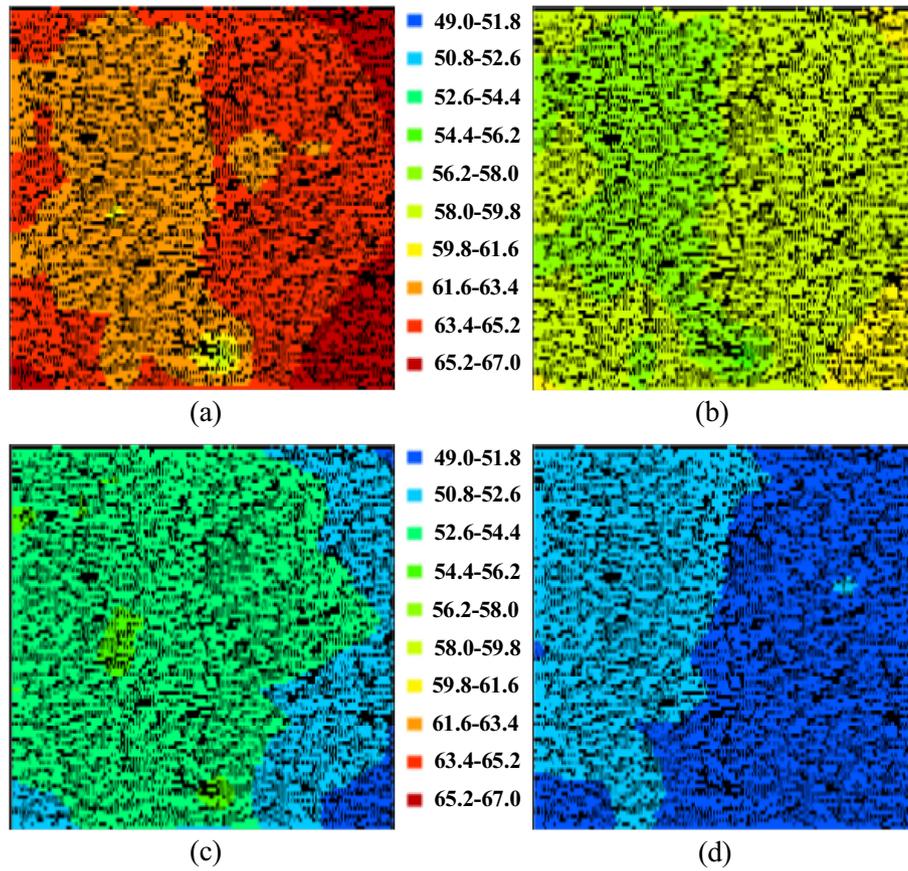


Fig. 2. Temperature profiles (°C) for the s38584 benchmark circuit under four different workloads of (a) high profile, (b) medium profile, (c) low profile, and (d) near idle.

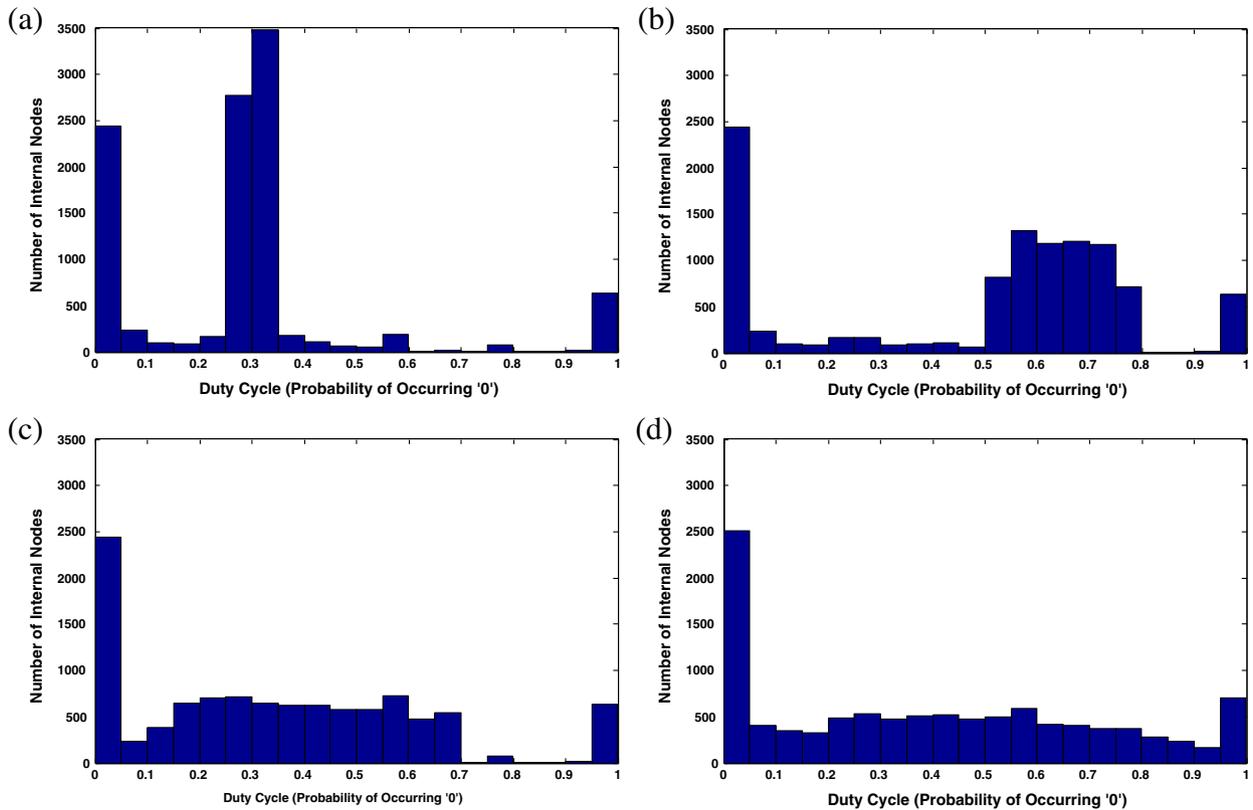


Fig. 3. The histograms of duty cycles of the internal nodes of s38714 benchmark for different workload conditions, (a) high load, (b) medium load, (c) low load, and (d) near idle.

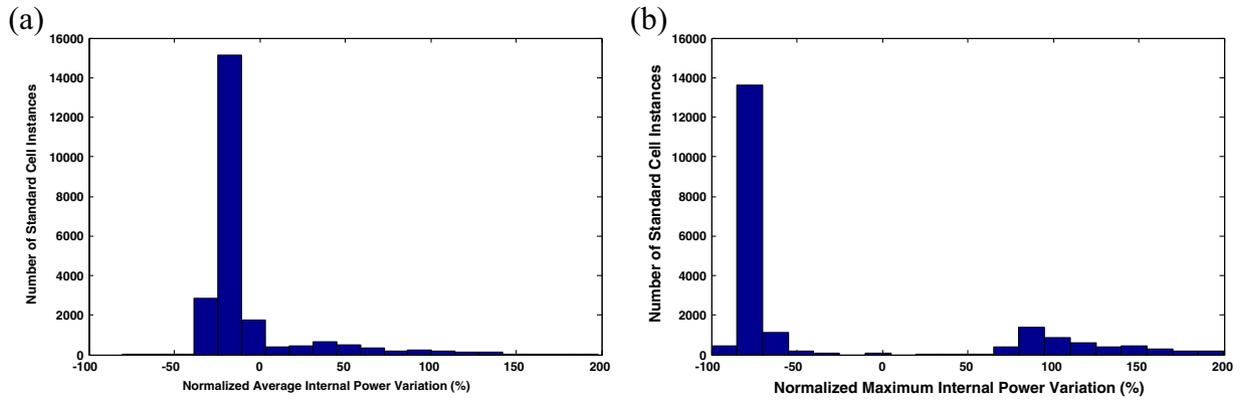


Fig. 4. (a) The average and (b) the maximum of internal power change for b21 circuit.

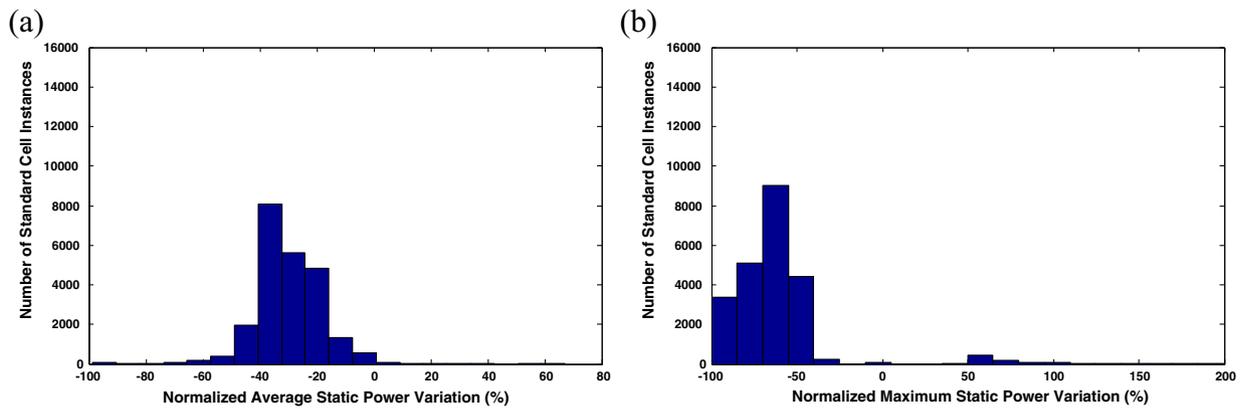


Fig. 5. (a) The average and (b) the maximum of static power change for b21 circuit.

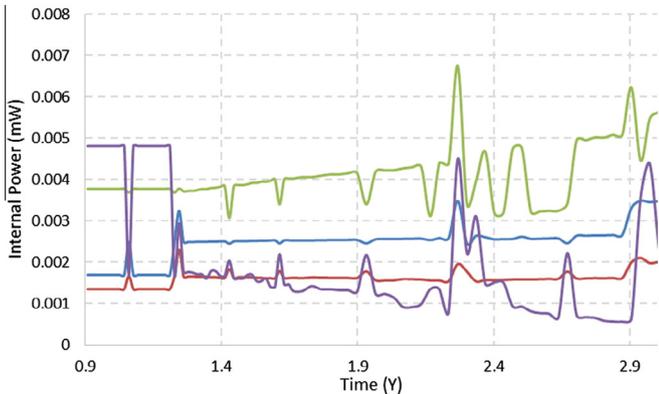


Fig. 6. Internal power for a time window of four cascaded NAND2X1 gates in b21 circuit.

the amount of the capacitances which some of them are voltage-dependent. Since the node voltage profiles are different for these gates, the corresponding capacitances for the gates become different again leading to different internal powers for these gates. These further stress out the importance of considering both the workload and die temperature dynamically for the circuit lifetime prediction.

4. Simulation framework and scenarios

In this section, we describe our aging aware simulation framework which considers the effect of both dynamic workload and

operating temperature in predicting the lifetime under NBTI-induced degradation. For this purpose, we need to have the standard cell library characterized at different threshold voltages and temperatures. Here, without loss of generality, 20 standards are selected cells for synthesizing the benchmarks. In this work, the operating temperature was assumed to vary between 300 °K and 400 °K with linear steps of 1° and the threshold voltage was swept in 100 steps from nominal value up to the degraded amount by 50%. The characterization was performed by obtaining the characteristics of the cells at each combination of temperature and threshold voltage. For this purpose Cadence Encounter Library Characterizer (ELC) tool was exploited. Based on these characterizations, a standard cell library bank with the size of 10,000 was formed. It should be noted the generation of this library bank should be performed once for each technology node.

The circuits were synthesized with the standard cell library with nominal threshold and operating temperature of 27 °C (300 °K) using Synopsys Design Compiler. Then, the netlists were used for the power and temperature analyses during the simulation. Here, in order to investigate the effect of dynamically considering the workload and the operating temperature on predicting the lifetime in the presence of NBTI effect, the simulation flow shown in Fig. 7 is used.

For the simulation, the lifetime is divided into N time periods where the boundaries of the time intervals are called as time-stamps. Here, the threshold voltage degradation is calculated at the end of each time interval. It should be noted that since the rate of the NBTI-induced threshold voltage degradation decreases as the time passes (see, e.g., [3]), we use the time intervals whose

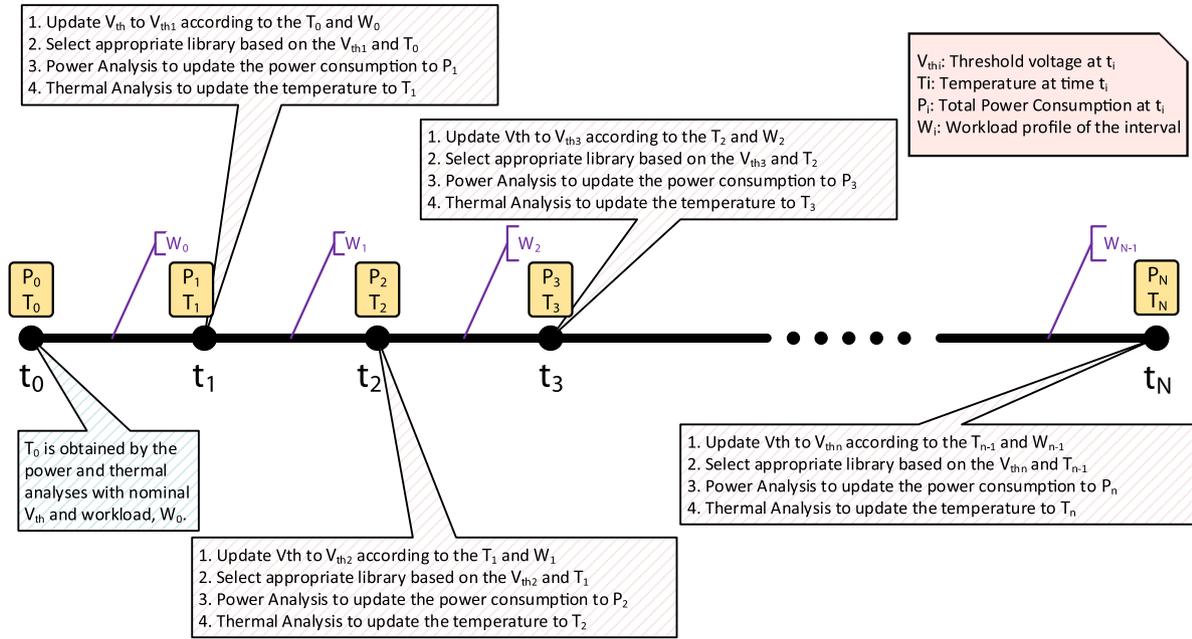


Fig. 7. Flow of the proposed simulation framework.

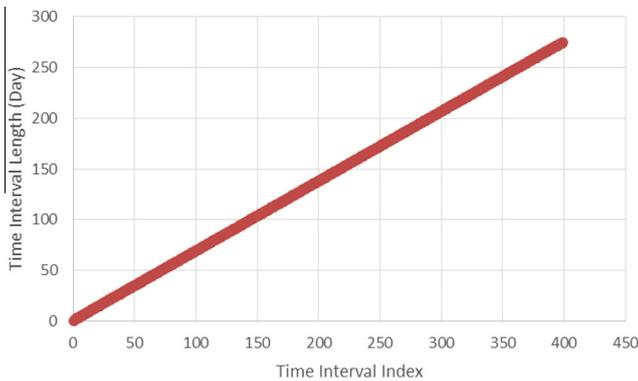


Fig. 8. The length of time intervals when 10 years lifetime divided into 400 intervals.

durations are increased by the time. In this work, the n th timestamp (t_n) is assumed to be obtained from:

$$t_n = t_{n-1} + 2n \cdot \frac{\text{lifetime}}{N(N+1)} \quad (4)$$

It should be noted that however, any other relations could be used for selecting the N th interval length, the form given in Eq. (4) provides us with minimal simulation error and reasonable simulation time. To have an idea about the rate of time period changes, we have plotted the length of the time intervals assuming a lifetime of ten years divided into one hundred intervals in Fig. 8. At each timestamp t_i , based on the updated threshold voltage and operating temperature (the spatial thermal profile obtained from Cadence Encounter Power System (EPS)), the corresponding library is picked up from the library bank. In the next interval, the power analysis is performed by Cadence Encounter Power System (EPS) using the selected characterized standard cell library instead of nominal (original) library. Since the V_{th} in the library is changed, the power consumption of the cells in the synthesized netlist would be different from the amount in the previous interval. Then, based on the provided power report by EPS, the thermal

analysis is performed by EPS to update the die temperature to its new value. In other words the EPS exploits the characterized standard cell libraries to adaptively update the power and temperature of each instance of standard cells of the circuit. The process is continued till reaching the end of the simulation time (10 years in this study). The timing degradation for the circuit is obtained at the end of the simulation time. More specifically, the simulation starts at t_0 with the nominal threshold voltage (V_{th0}) assuming the starting operating temperatures (T_0 's) which are determined by some simulations (for the given workload profile) before starting the actual simulation. At the end of the first time intervals (t_1), the threshold voltages of the standard cells are updated using Eq. (1) based on the assigned workload profile (W_0) and the operating temperatures at the beginning of that interval (T_0 's). Based on the updated threshold voltages (V_{th1} 's) and T_0 's, the corresponding cell library is selected from the library bank which is used along with W_0 in the power and thermal analyses are performed to update the operating temperatures (T_1 's). The same procedure is repeated until the end of the simulation of the circuit for desired time (see Fig. 7). Obviously, decreasing the time intervals increases the accuracy of the results at the price of enlarging the simulation time.

To the best of our knowledge, there was no experimental data for the validation of the results experimentally. As the next best available option for determining the accuracy of the proposed approach, four different simulation scenarios were invoked where depending on the scenario some of the mentioned steps were not executed. In the first scenario (denoted by S1) both the application workload and the operating temperature were simply assumed to be constant. The temperature for this scenario was determined based on running the simulator for each circuit when the medium load workload was considered. Then, the spatial thermal profile was used for the circuit lifetime prediction. In this study, for the comparison purpose, the 10 year changes of the threshold voltages for the transistors were calculated based on the thermal profile. These changes were used to calculate the timing degradation of the circuit. In fact, in this scenario, there was one time interval of ten years. In the second scenario (S2), a dynamic workload was considered while the operating temperature was assumed to be constant (obtained by running the simulator for each circuit when the medium load workload for a given time). The workload was

assumed to vary between high load (HL), medium load (ML), low load (LL) and near idle (NI). The average activity of the primary inputs in these profiles was 50%, 40%, 30%, and 10% respectively. Here, without loss of generality, we assumed that the workload variation profile followed the ML, HL, NI, and NL workload pattern which were repeated in consecutive time intervals. The simulation under the third scenario (S3) was performed assuming a fixed (medium load) workload while considering the dynamic changes of the temperature. Finally, the fourth simulation scenario (S4), as the more accurate approach, incorporated dynamic variations of both the workload and operating temperature using the flow shown in Fig. 7. As the last point, it should be noted that the process variation affects the zero time circuit performance (prior actual circuit operation). Since the focus of our work is on the aging and lifetime of the circuit after its actual prediction with the objective of investigating the importance considering the die temperature and workload on the circuit lifetime, the effects of process variation are not included in simulations. The investigation performed in this work can be started with any pre-specified (zero time) circuit performance.

5. Results and discussion

In this section, we investigate the impact of considering both the operating temperature and workload in predicting the circuit lifetime in the presence of NBTI phenomenon using the simulation framework described in the previous section. For this investigation, a set of seven circuits from ISCAS'89 and ITC'99 benchmark suites were considered. Since the spatial temperature variation in small circuits is not significant, the circuits with larger areas from each suite were selected. The benchmarks were synthesized using the 45 nm Nangate standard cell library [22]. We studied the circuit timing degradation for a period of ten years which was partitioned into 400 time intervals (see Fig. 8). Obviously, the smaller the interval is the higher the accuracy and the simulation time will be. Our results showed that the intervals obtained from Eq. (4), could provide a good accuracy for this approach of lifetime prediction. All the circuits were simulated with the four scenarios (S1, S2, S3 and S4) stated in Section 4. To obtain the delays of the circuit, the tool Cadence SOC Encounter has been utilized.

The results for the time-zero delay and NBTI-induced degraded delay for each circuit under these four scenarios are presented in Table 1. For example, in the case of s35932 circuit, a dynamic workload and a fixed temperature were considered in S2 scenario. In this scenario, the considered operating temperature was obtained by running the simulator for a given amount of time for each circuit when the medium load profile was applied to the circuit. Please note that the medium workload normally leads to higher operating temperature than those of the low and idle profiles. In the case of S4, the workload is the same as S2 while the temperature is determined dynamically which could be sometimes higher and sometimes lower than that of S2. Therefore, this has led

to a lower delay degradation for S4 for s35932 circuit. In the case of S1, fixed workload and temperature were assumed whereas for S3 the temperature was dynamically determined and the workload was the same as that of S1. Since the temperature sometimes would be lower than that of S1, the delay degradation is less in the case of S3. Owing to the fact that higher activity profile alone does not necessarily lead to higher delay degradation (because the circuit structure may be in a way that the nodes in the critical path have low duty cycles), one may not expect a higher delay degradation whenever there is a higher activity profile. In addition, the increase in the threshold voltage causes lower active leakage power and hence lowering the temperature. Due to the cross-dependencies between different parameters, no specific delay degradation trend may not be expected for the circuits when comparing different scenarios. For the results provided in Table 1 of the other circuit, similar justifications may be provided. The investigations performed instantiate considering both dynamic temperature and workload in predicting the circuit lifetime.

A comparison between the delay degradations of these scenarios is plotted in the bar chart shown in Fig. 9. The results are based on the differences between the results of the first three scenarios and that of the fourth one. As the results reveal that the maximum difference between the predicted timing degradation of S4 with those of the others ranges from -135% to $+98\%$. The amount of the differences is a function of the circuit and workload profile. Noting the fact that the S4 scenario considers more dynamic information for predicting the lifetime, its predicted time degradation should be more accurate implying much more accuracy for this approach of lifetime prediction.

The histograms in Figs. 10 and 11 depict the threshold voltage increases of the gate instances in b15 (as an example of a small size benchmark) and b21 (as an example of a large size benchmark) circuits for all four scenarios respectively. For the circuit b15 (b21), the threshold voltage changes range from 0.8 (3.5)% to 15.3 (65.9)% in the case of the S1 while they span from 1.9 (2.8)% to 36.6 (54.0)% in the case of the S4. It should be noted that, in the case of S1, the simulator predicts the maximum change of the threshold voltage change to 15.3%, for the circuit b15, which is about 21.3% lower than that of the S4, and hence, the circuit lifetime will be overestimated if the S1 (with medium load profile) is used for the prediction. Along the same line of thought, the other results also could be justified.

Referring to Fig. 9, one observes that, except for the circuit s38417, using the S1 causes a less delay degradation over ten years (an overestimation of the circuit lifetime). In the case of s38417, it seems that the impact of the temperature is more than that of the workload. Our results show that the predicted temperature for the S1 is higher leading to shorter circuit lifetime. Apparently, using the high load profile leads to a more delay degradation.

Also, for b15 circuit, both the S2 and S4 predicts almost the same lifetime for the circuit. This originates from the fact that the temperature variation under different workloads is small and also, the total impact of the NBTI on the critical path of this circuit is small (see Table 1). For the case of the S3, a large population of the cells see the minimum threshold voltage degradation, and hence, the delay degradation in this case is lower than that of the S4. The cells on the critical path have the most impact on the timing degradation if their threshold voltage changes are high.

In the case of the circuit b21, again considering the fact that most of the threshold voltage changes occur in the lower range of the changes, the predicted lifetime will be considerably higher than those of the other scenarios. For this circuit, while for both cases of the S2 and S3 about the same number of the cells experience the largest threshold voltage changes, for the former (latter) scenario a high fraction of the cells see about 40% (5%) of the changes, and hence, the S2 leads to more timing degradation.

Table 1

The nominal delay and degraded delay of the considered benchmarks after expected lifetime under 4 different scenarios.

Benchmark	Gate	Delay (ns)	Δ Delay (%)			
			S1	S2	S3	S4
b15	7060	3.08	0.32%	0.97%	0.32%	0.97%
b17	23,635	4.694	8.99%	27.46%	41.33%	49.32%
b20	23,680	11.598	10.17%	42.00%	20.45%	21.02%
b21	23,493	12.987	0.87%	10.42%	9.00%	4.44%
s35932	9125	0.663	0.30%	10.56%	0.15%	7.69%
s38417	10,223	1.266	15.80%	10.27%	15.48%	15.32%
s38584	11,306	2.079	25.59%	50.60%	36.75%	36.22%

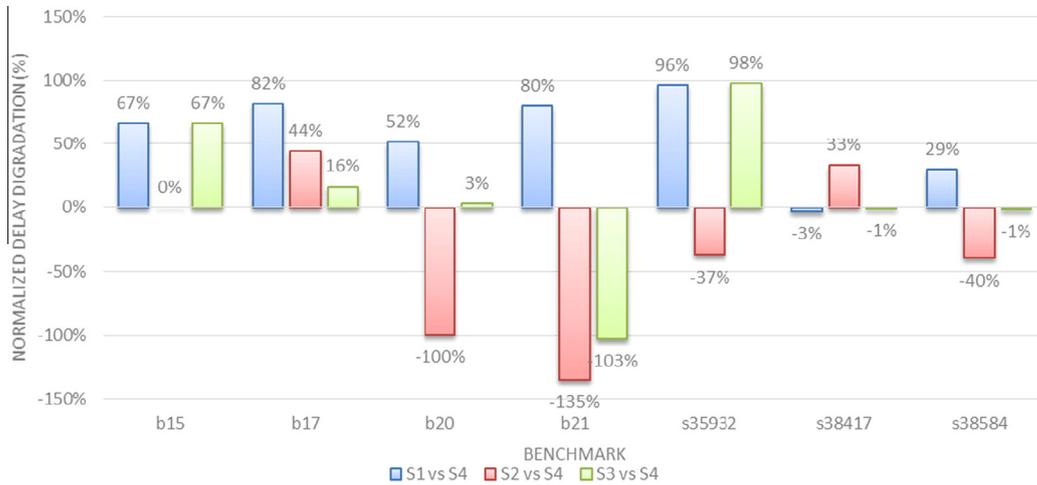


Fig. 9. Comparison of the simulation results under static (S1) and semi-static (S2 and S3) operating condition with proposed dynamic simulation framework (S4).

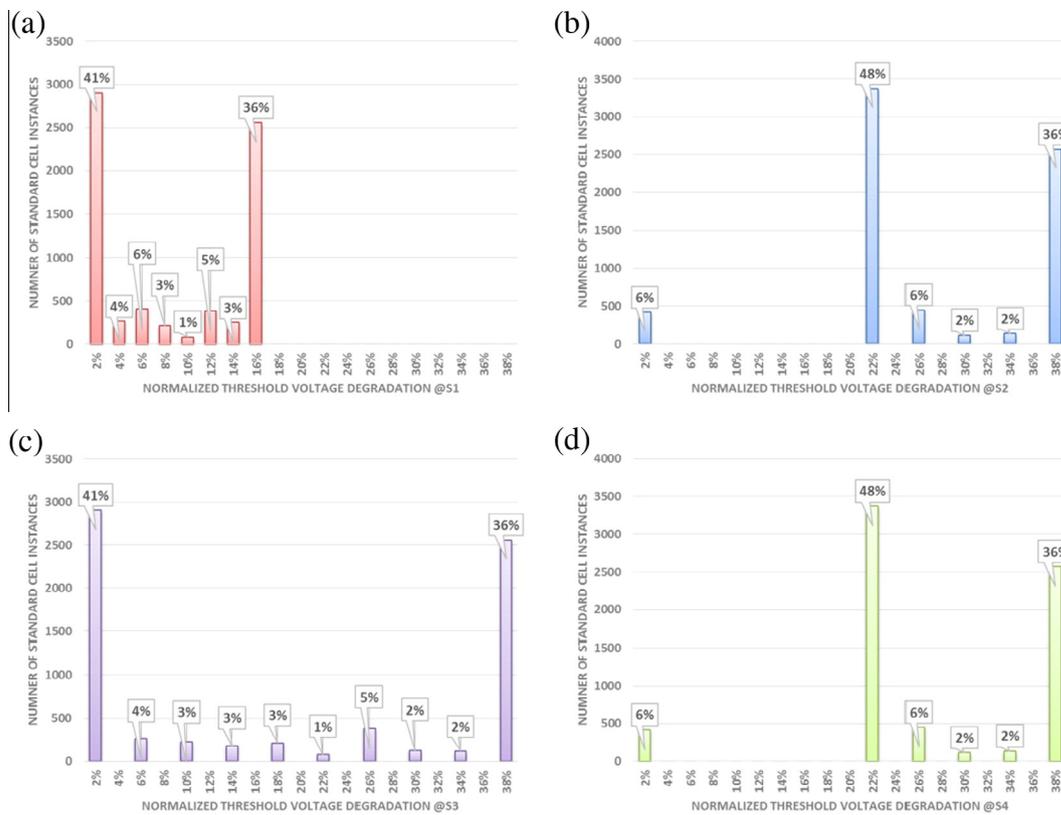


Fig. 10. The distribution of normalized threshold voltage degradation of the gate instances in b15 benchmarks under (a) S1, (b) S2, (c) S3, and (d) S4 scenarios.

Also, it should be noted that, in the case of the S4, the high populated threshold voltage changes are for the changes lower than those of the case of the S3 while the other high populated threshold voltage changes occurs in higher threshold voltage changes. As a result, both the S3 and S4 lead to about the same delay degradation. Lastly, note that although more or less the same trends are observed in the cases of both circuits, the differences in the behaviors are observed which are attributed to the differences in the topology of the circuits.

Finally, the averages of the threshold voltage changes (ΔV_{th}) for all the cell instances are summarized in Table 2. The figures in the table reveal that, for the case of the dynamic operating condition, the mean of the threshold voltage changes will be higher than that of the static

case S1 with the assumption of the medium workload profile for all the circuits. For this scenario, if we consider the high workload profile, the mean becomes higher. When comparing the dynamic and the semi-static case of S2, except for the circuit b17 (due to the underestimate temperature prediction), the mean is higher for the latter case which assumed a constant operating temperature while assuming a dynamic workload. Finally, for the semi-static case of S3 where the workload profile was assumed constant and the dynamic variation of the die temperature was considered, the mean was always smaller than that of the S4 case. These observations emphasize the importance of considering the dynamic operating temperatures for preventing under- or over-estimation of the circuit lifetime in the presence of the BTI phenomena.

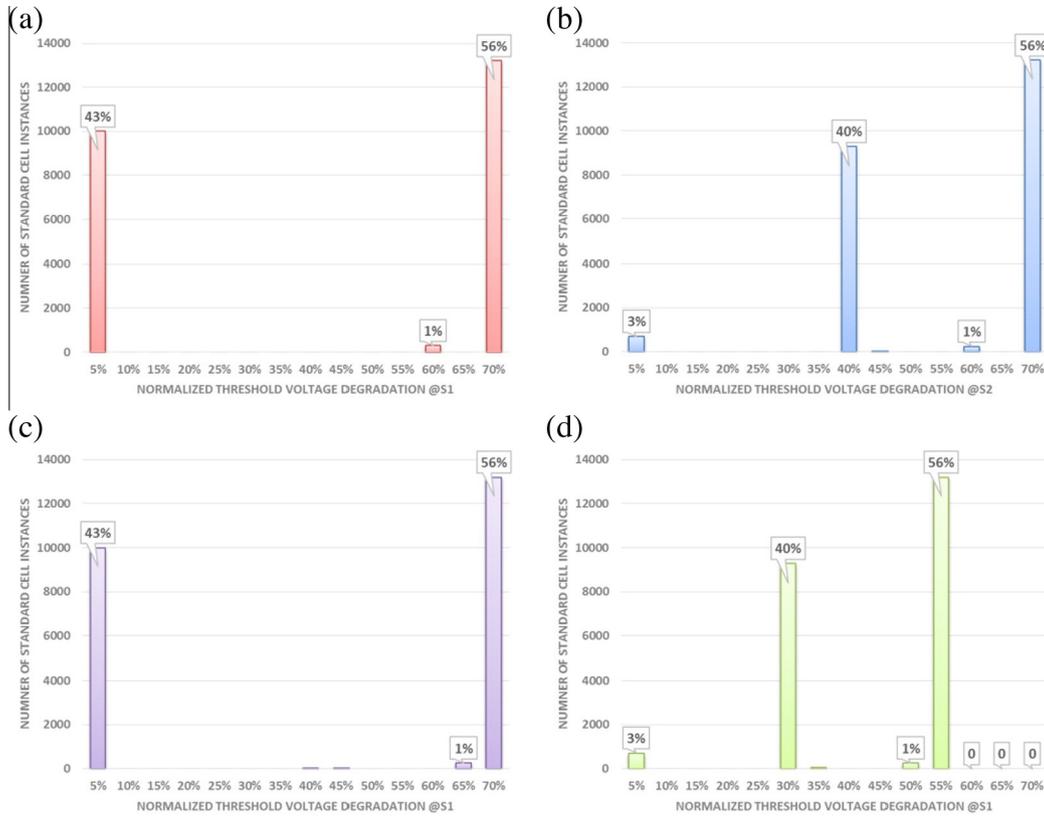


Fig. 11. The distribution of normalized threshold voltage degradation of the gate instances in b21 benchmarks under (a) S1, (b) S2, (c) S3, and (d) S4 scenarios.

Table 2

Average threshold voltage degradation among the standard cell instances in considered benchmarks.

Benchmark	Mean of the ΔV_{th}			
	S1	S2	S3	S4
b15	7.4%	26.6%	18.2%	26.0%
b17	15.0%	42.1%	33.0%	47.4%
b20	15.8%	46.3%	19.8%	39.2%
b21	39.6%	50.3%	41.5%	41.8%
s35932	6.6%	26.5%	15.3%	23.7%
s38417	5.5%	29.7%	11.2%	22.4%
s38584	13.3%	37.5%	28.7%	30.2%

In order to study the trend of threshold voltage change in dynamic condition, as an example, we have plotted the normalized threshold voltage change for a standard cell instance in b20 benchmark with high activity inputs in two scenarios of S1 and S4 in Fig. 12. The S1 scenario represents Eq. (2) while under S4 scenario the dynamic variations of both die temperature and workload were considered. The overall trends of the threshold voltage with time remain similar although, the degradation rate is higher in the case of S4.

6. Conclusion

In this paper, a simulation framework for studying the NBTI-induced delay degradation in digital circuits was discussed. The framework had the ability to incorporate both the workload and die temperature variations during the circuit operation. We used this framework to evaluate the importance of considering interwoven effects of the workload and operating temperature

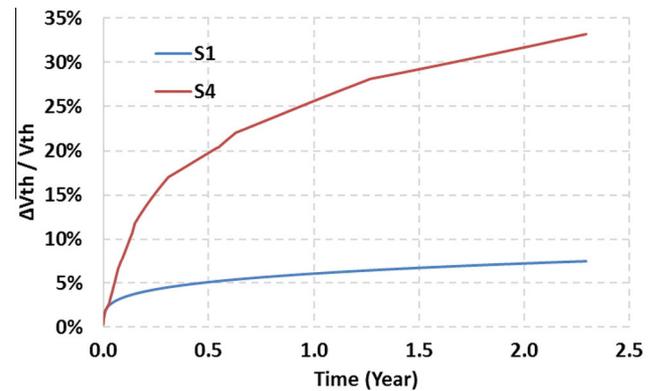


Fig. 12. Normalized threshold voltage change for a standard cell instance in b20 benchmark with high activity inputs.

when predicting the lifetime degradation in the presence of the NBTI phenomenon. The evaluation was performed by considering the four cases of dynamic (both temperature and workload were updated dynamically), semi-static (either of temperature and workload was updated dynamically), and static (no updating is performed) scenarios. For the evaluation, circuits from ISCAS'89 and ITC'99 benchmark suites when synthesized using a 45-nm technology were considered. The results revealed that the predicted timing degradation had errors ranging from -135% to +98% when the dynamic operating conditions were not considered.

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