Battery-Powered Digital CMOS Design

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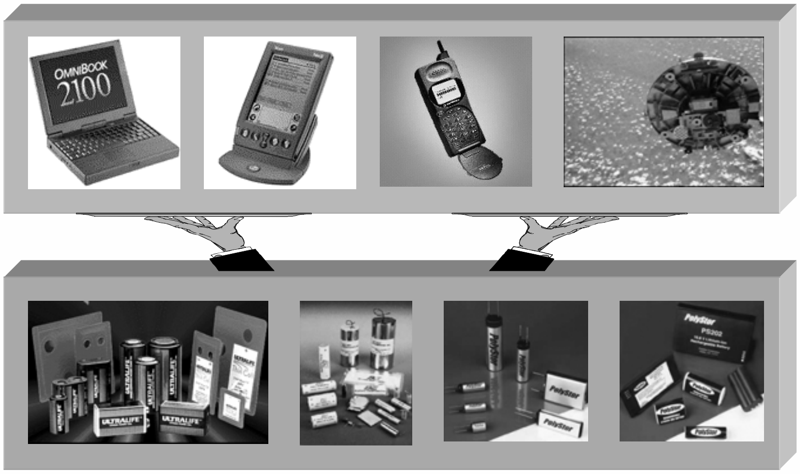
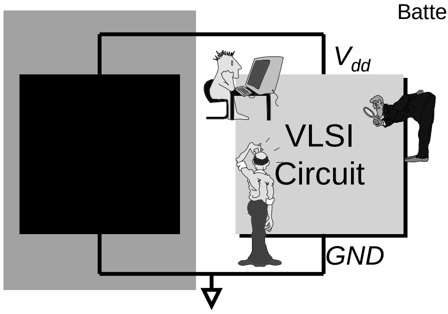
Motivation

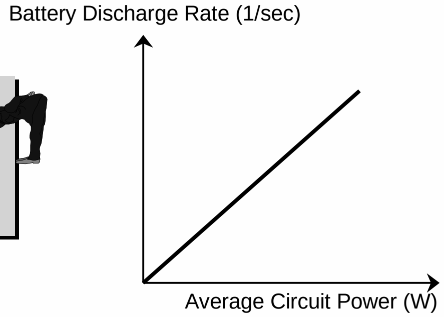
Extending the *battery service life* of battery-powered micro-electronic devices is a primary design objective



Conventional System Model

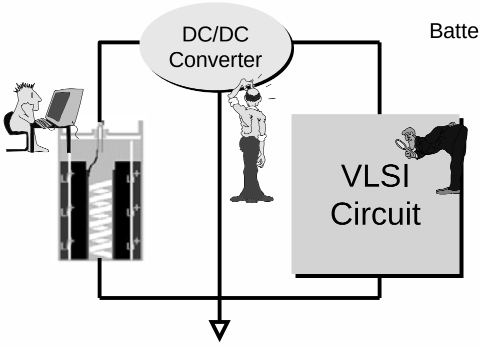
- ❑ Existing low power design methodologies and approaches target power consumption in the VLSI circuit
- ❑ The battery system is assumed to be an ideal source that delivers a fixed amount of energy
- ❑ Common perception is that the *battery discharge rate* (i.e., the inverse of the battery service life) is linearly related to the average power consumption in the VLSI circuit

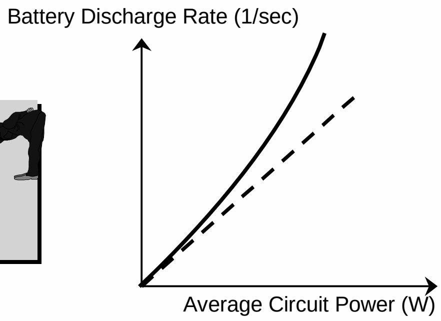




Integrated Battery-Hardware Model

- ❑ In reality, the battery discharge rate is super-linearly related to the average power consumption in the VLSI circuit





Common Battery Types

Type	Energy	Applications
Miniature	100 mWh~2 Wh	Electric watches, calculators, implanted medical devices
Batteries for portable equipment	2~100 Wh	Flashlights, toys, power tools, portable radio and television, mobile phones, camcorders, lap-top computers
SLI Batteries (starting, lighting and ignition)	100~600 Wh	Cars, trucks, buses, tractors, lawn mowers
Vehicle traction batteries	20~630 kWh	Fork-lift trucks, milk floats, locomotives (submarines)
Stationary batteries	250 Wh~5 MWh	Emergency power supplies, local energy storage, remote relay stations
Load leveling batteries	5~100 MWh	Spinning reserve, peak shaving, load leveling

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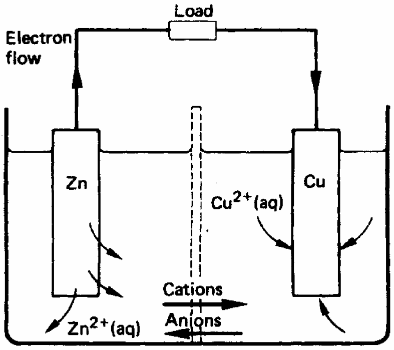
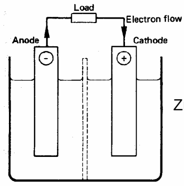
How Batteries Work: An Example

A Galvanic Cell:



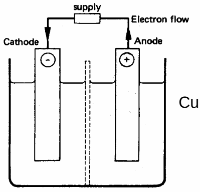
Discharge:



$Zn(s)|Zn^{2+}(aq),m_1||Cu^{2+}(aq),m_2|Cu(s)$

$$Zn(s)+Cu^{2+}(aq),m_2 \rightarrow Zn^{2+}(aq),m_1+Cu(s)$$

Charge:



$Cu(s)|Cu^{2+}(aq),m_2||\ Zn^{2+}(aq),m_1|Zn(s)$

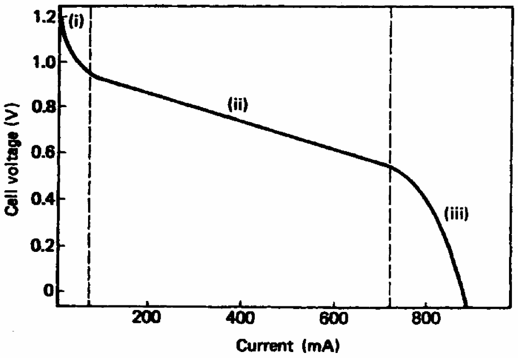
$$Zn^{2+}(aq),m_1+Cu(s) \rightarrow Zn(s)+Cu^{2+}(aq),m_2$$

Battery Characteristics

- ❑ Electrochemical capacity
  - ⇨ Practical capacity Q_p is lower than the theoretical electrochemical capacity
  - ⇨ Mass-based specific capacity (Ah/Kg) and Volume-based specific capacity (Ah/dm^3)
- ❑ Energy (rated capacity)
  - ⇨ The practical available energy E_p is dependent on the manner in which the cell is discharged (I.e., the discharge current)
- ❑ Power (rated power)
  - ⇨ Specifies whether or not a battery is capable of sustaining a large current drain without undue polarization
  - ⇨ Cells employing the same chemical system can be designed for either high power or high energy

Battery Polarization

Typical polarization curve for an electrochemical cell



Region (i): Electrode polarization overvoltage, usually associated to a large extent with one of the two electrode processes
Region (ii): *iR* polarization caused by the internal resistance of the cell
Region (iii): *iR* polarization combined with further electrode polarization caused by depletion of electroactive materials at the electrode surface

Battery Performance Criteria

- Battery testing and specifications
  - Useful life test (this test of a practical primary battery is determined principally by the nature of its discharge pattern)
  - Other tests include, storage (shelf life) test, assessment under conditions of environmental and mechanical stress, cell behavior under conditions of continuous short circuit, cell behavior after complete discharge, etc.
- Rechargeable systems
  - Cycle life (the number of times a cell can undergo a charge/discharge sequence before its performance is degraded to below some specified threshold)
  - Battery must have a satisfactory rate of charge acceptance
- Thermal management
  - Maximum working temperature, above which corrosion and other irreversible destructive processes are very rapid
  - Minimum working temperature, below which the electrolyte has too high a resistance or may undergo a phase change

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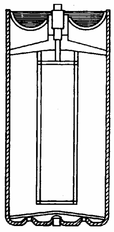
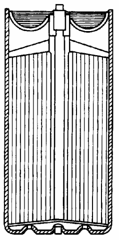
Typical Battery Structures

High-energy structure **High-power structure** → **Spiral wound ('jelly roll') structure**





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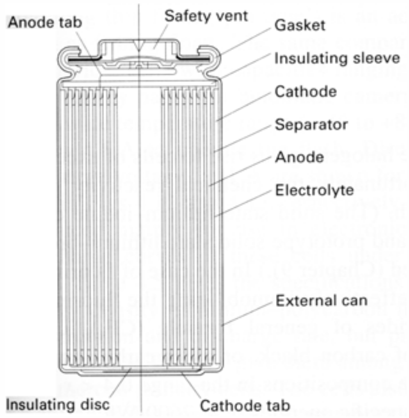
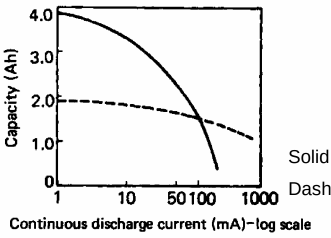


Discharge performance

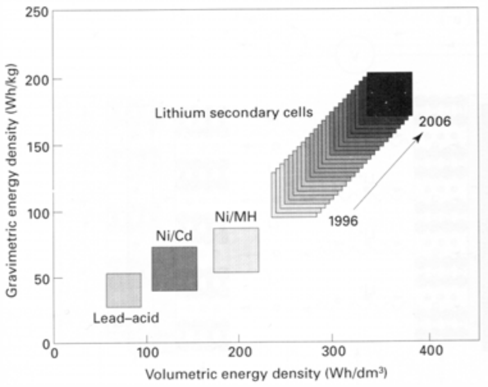


Solid: High-energy structure

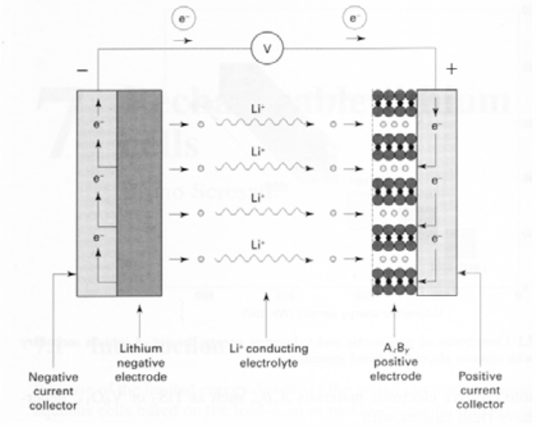
Dashed: High-power structure

Rechargeable Batteries

Comparison of gravimetric and volumetric energy density of lithium secondary cells with aqueous electrolyte-based systems

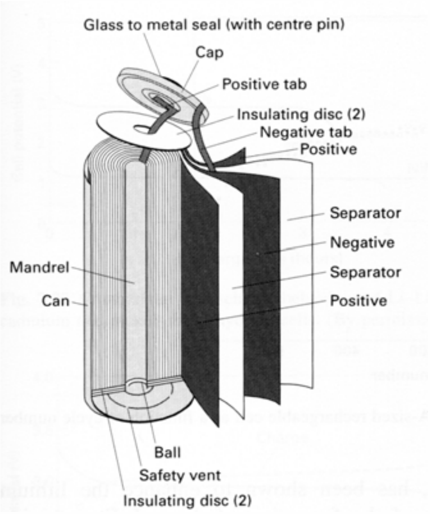


Battery Discharge Diagram



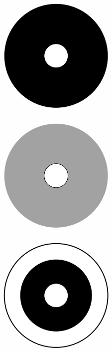
$$x\mathrm{Li(s)}+\mathrm{A}_z\mathrm{B}_y\mathrm{(s)} \underset{\text{charge}}{\overset{\text{discharge}}{\rightleftharpoons}} \mathrm{Li}_x\mathrm{A}_z\mathrm{B}_y\mathrm{(s)}$$

Typical Structure



Relevant Battery Characteristics

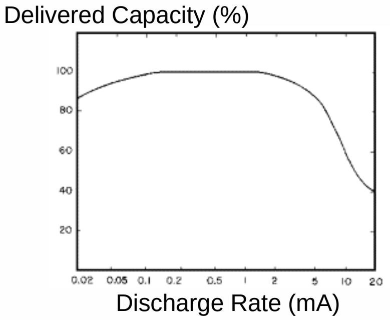
- ☐ The output voltage of a battery decreases as the battery is discharged
- ☐ A battery cell discharged at high current rate may lose capacity due to Cathode Freeze-Over; The amount of capacity loss is a function of discharge current rate
- ☐ A battery cell discharged at very low current rate may lose capacity due to self-discharge



Unused Cathode

Nominal Rate Discharge

High Rate Discharge



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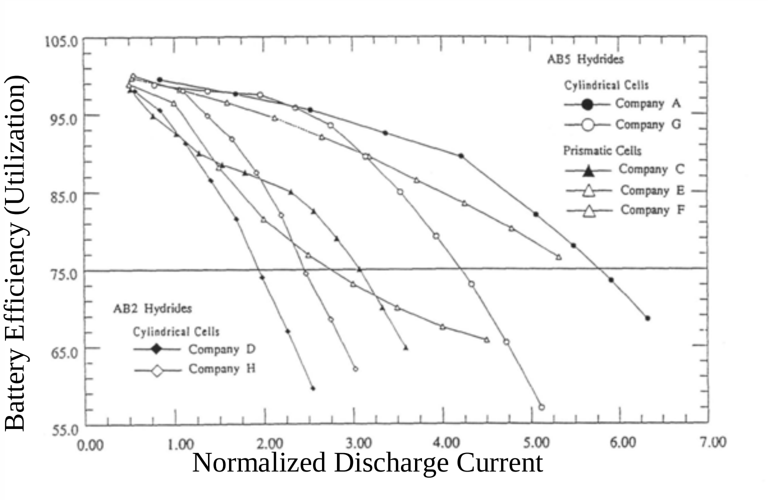
Rate Capacity of Commercial NiMH Batteries



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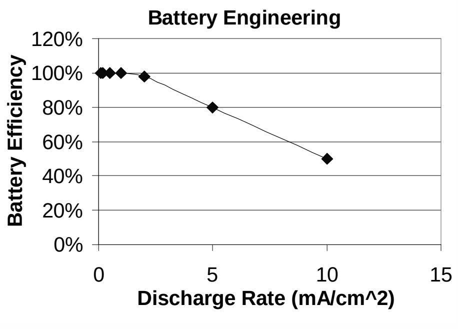
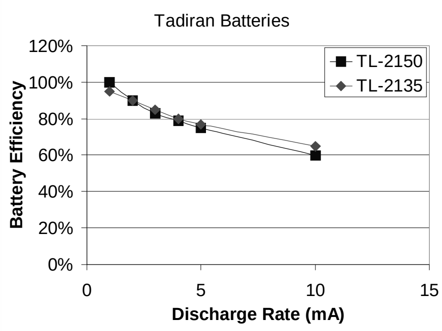
Rate Capacity of Commercial Lithium Batteries





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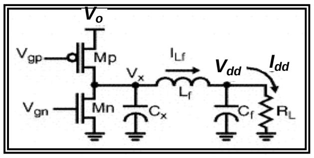
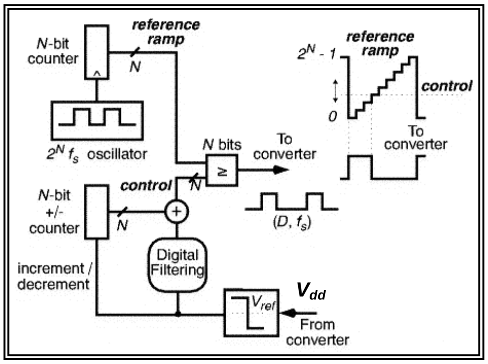
DC/DC Converter



(a) Buck Converter



(b) Control Circuit

V_0 : Battery output voltage

I_0 : Average battery output current (over time $N.T$)

V_{dd} : VLSI circuit supply voltage

I_{dd} : Average VLSI circuit supply current (over time $N{\cdot}T$)

η : Efficiency of DC/DC converter

$$\eta \cdot V_0 \cdot I_0 = V_{dd} \cdot I_{dd}$$

Actual Current

The *actual discharge current* of the battery, after considering the capacity-rate effect, is:

$$I_0^{act} = I_0 / \mu, \quad 0 \le \mu \le 1$$

μ : the *battery efficiency,* is a function of I_0 :

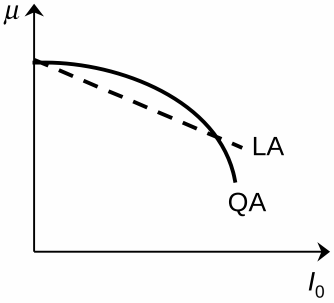
$$\mu = f(I_0)$$

We can approximate ***f*** by using a:
Linear Approximation (LA):

$$\mu = 1 - \beta \cdot I_0$$

Quadratic Approximation (QA):

$$\mu = 1 - \gamma \cdot I_0^2$$



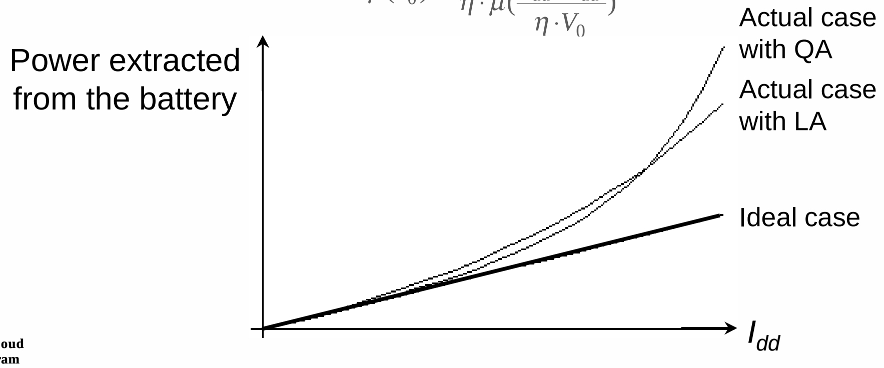
Ideal and Actual Power Dissipation

Given a fixed supply voltage V_{dd}, power extracted from the battery is:

$$P^{ide} = V_0 \cdot I_0 = \frac{V_{dd} \cdot I_{dd}}{\eta}$$

When we consider the electro-chemical characteristics of the battery, we have:

$$P^{act} = V_0 \cdot \frac{I_0}{\mu(I_0)} = \frac{V_{dd} \cdot I_{dd}}{\eta \cdot \mu(\frac{V_{dd} \cdot I_{dd}}{\eta \cdot V_0})}$$



Observation I

For the same voltage level, the actual power dissipation is a super-linear function of the current consumed in the VLSI circuit.

The Actual Power Dissipation

p_1 : The profile (probability density function) of I_{dd}
p_2 : The profile (probability density function) of I_0
p_1 and p_2 have the same form, but different scale

Ideal power extracted from the battery:

$$P^{ide} = \int_{I_{0,MIN}}^{I_{0,MAX}} V_0 \cdot I_0 \cdot p_2(I_0) dI_0$$

$$= V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} I_0 \cdot p_2(I_0) dI_0 = V_0 \cdot I_0^{ave}$$

Actual power extracted from the battery:

$$P^{act} = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} \frac{I_0}{\mu(I_0)} \cdot p_2(I_0) dI_0$$

Actual Power Using LA and QA

Linear Approximation (LA):

$$P^{act} = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} \frac{I_0}{1 - \beta \cdot I_0} \cdot p_2(I_0) dI_0$$

Quadratic Approximation (QA):

$$P^{act} = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} \frac{I_0}{1 - \gamma \cdot I_0^2} \cdot p_2(I_0) dI_0$$

Two Distributions with the Same Mean

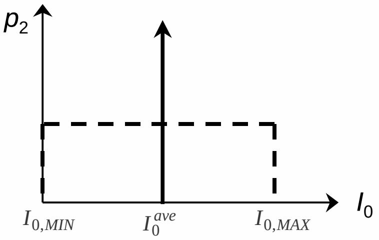
Uniform Distribution:
maximizes the actual power

$$p_2(I_0) = \begin{cases} \dfrac{1}{I_{0,MAX} - I_{0,MIN}}, & I_{0,MIN} \le I_0 \le I_{0,MAX} \\ 0, & otherwise \end{cases}$$

$$\frac{I_{0,MIN} + I_{0,MAX}}{2} = I_0^{ave}$$

***δ*-function Distribution:**
minimizes the actual power

$$p_2(I_0) = \delta(I_0 - I_0^{ave})$$



MAX and MIN Actual Power Using LA

$$P_{MAX}^{act} = \frac{V_0}{(I_{0,MAX} - I_{0,MIN})} \cdot \frac{\beta(I_{0,MIN} - I_{0,MAX}) + \ln(\dfrac{1-\beta \cdot I_{0,MIN}}{1-\beta \cdot I_{0,MAX}})}{\beta^2}$$

$$P_{MIN}^{act} = V_0 \cdot \int_{I_{0,MIN}}^{I_{0,MAX}} \frac{I_0}{1-\beta \cdot I_0} \cdot \delta(I_0 - I_0^{ave}) dI_0 = \frac{V_0 \cdot I_0^{ave}}{1-\beta \cdot I_0^{ave}}$$

MAX and MIN Actual Power Using QA

$$P_{MAX}^{act} = \frac{V_0}{(I_{0,MAX} - I_{0,MIN})} \cdot \frac{\ln(\frac{1-\gamma \cdot I_{0,MIN}^2}{1-\gamma \cdot I_{0,MAX}^2})}{2\gamma}$$

$$P_{MIN}^{act} = \frac{V_0 \cdot I_0^{ave}}{1-\gamma \cdot (I_0^{ave})^2}$$

Battery Service Life and Discharge Rate

Battery Service Life (BSL):

$$BSL = \frac{CAP_0}{P^{act}}$$

Battery Discharge Rate (BDR):

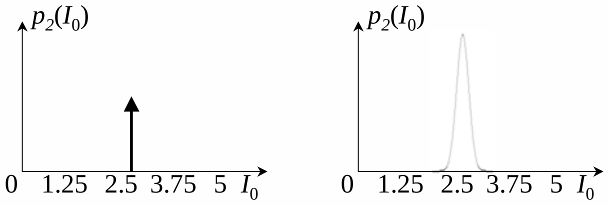
$$BDR = \frac{1}{BSL}$$

A Quantitative Example

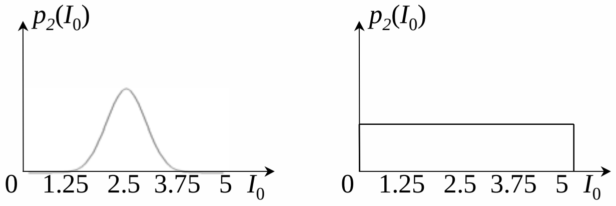
Consider a battery with 36KJ nominal capacity and a 4-volt nominal output voltage:

Parameter	Value
V_0	4V
$I_{0,MIN}$	0A
$I_{0,\ MAX}$	5A
β	0.12 (1/A)
γ	0.024 (1/A^2)
CAP_0	36KJ (2.5AH)
I_0^{ave}	2.5A

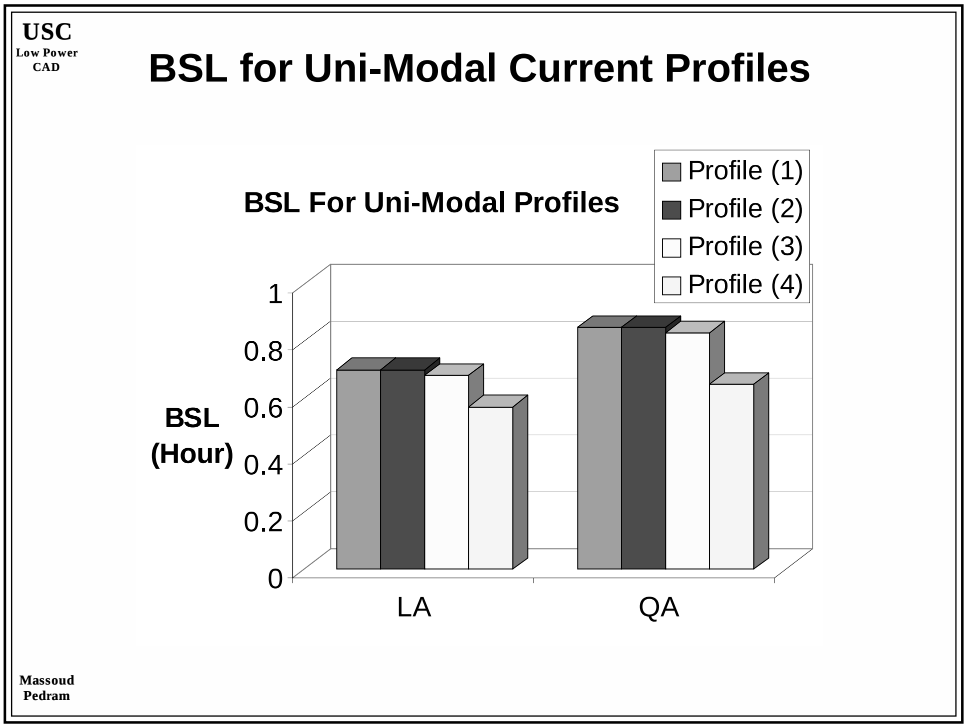
Current Profiles for Uni-Modal Operation



(1) Pulse (2) Normal (σ=0.1)



(3) Normal (σ=0.5) (4) Uniform



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BSL for Uni-Modal Current Profiles

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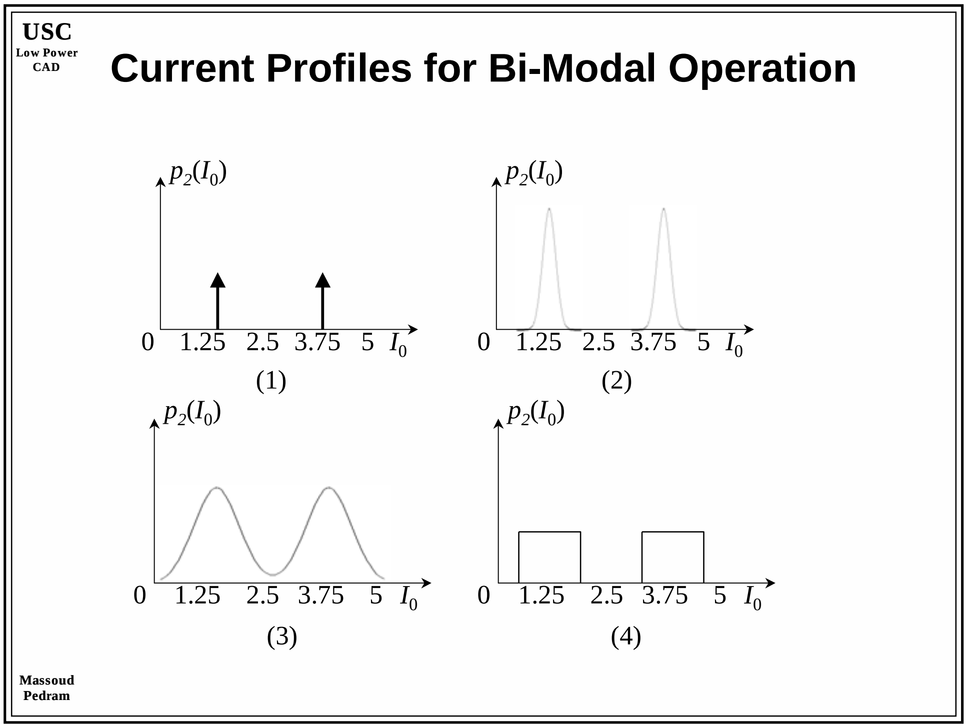

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Current Profiles for Bi-Modal Operation

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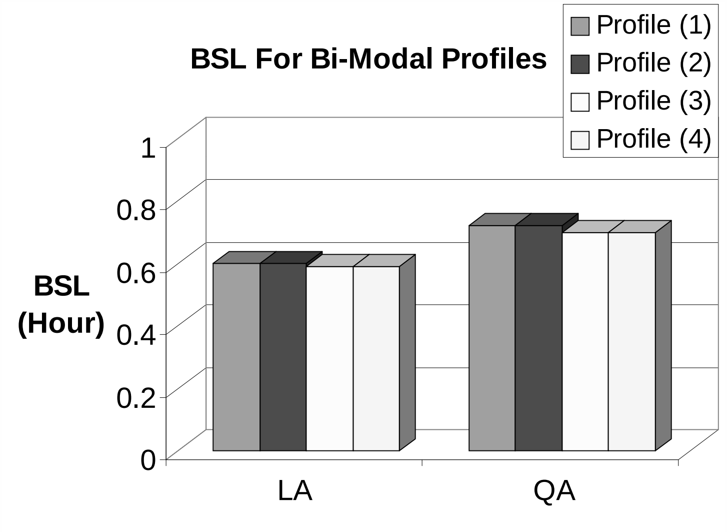
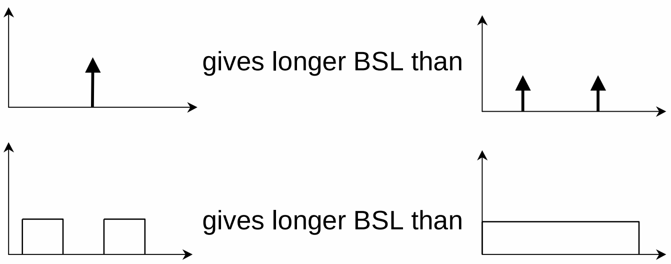
BSL for Bi-Modal Current Profiles



Conclusions from the Example

- ❑ The maximum BSL occurs by using the δ-function distribution
- ❑ The minimum BSL occurs by using the uniform distribution
- ❑ There is a significant increase (20%-30%) in BSL from the worst case to the best case
- ❑ Comparing uni-modal and bi-modal power distributions, we observe that:



gives longer BSL than

gives longer BSL than

Observation II

Even with identical mean value, different current profiles (i.e., current density functions) may result in very different actual power dissipations.

Battery Discharge (BD)

Definition:

$$BD = \frac{E^{act}}{CAP_0}$$

Actual battery energy dissipation per operation:

$$E^{act} = \frac{E^{ide}}{\mu(I_0)}$$

The circuit energy dissipation per operation:

$$E^{ide} = \tfrac{1}{2} C_{sw} \cdot V_{dd}^2$$

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Battery Discharge (cont.)

The average circuit current per operation:

$$I^{ide} = \frac{E^{ide}}{V_{dd} \cdot T} = \frac{C_{sw} \cdot V_{dd}}{2T}$$

The average battery current per operation:

$$I_0 = \frac{C_{sw} \cdot V_{dd}^2}{2T \cdot \eta \cdot V_0} = \frac{k \cdot V_{dd}^2}{T}$$

The Battery Discharge as a function of V_{dd} (using the Linear Approximation for $\mu(I_0)$):

$$BD = \frac{C_{sw}}{2 \cdot CAP_0} \cdot \frac{V_{dd}^2}{(1 - \beta \cdot k \cdot V_{dd}^2 / T)}$$

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BD-Delay Product Using LA

Delay equation for today's CMOS technology

$$t_d = m \frac{V_{dd}}{(V_{dd} - V_{th})^{\alpha}}, \qquad 1 < a \leq 2$$

The BD-Delay Product is:

$$BD\text{-}D = \frac{m \cdot C_{sw}}{2 \cdot CAP_0} \cdot \frac{V_{dd}^3}{(1 - \beta \cdot k \cdot V_{dd}^2 / T) \cdot (V_{dd} - V_{th})^{\alpha}}$$

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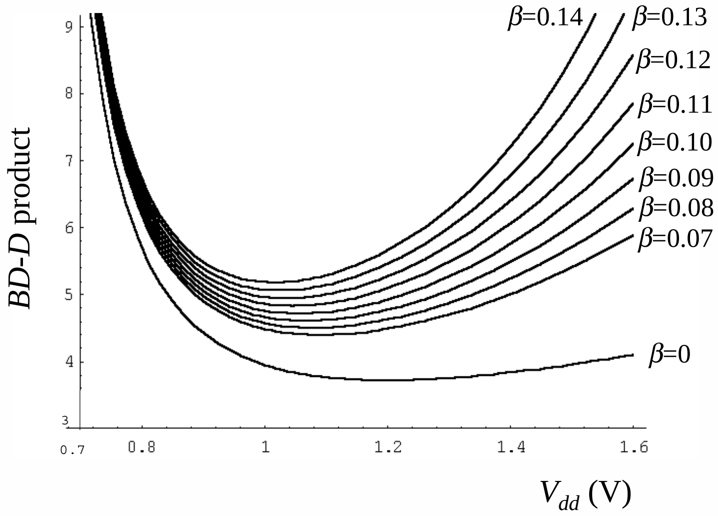
Case 1: Fixed Operation Latency

Assume T is fixed for all V_{dd} values.
Consider a VLSI circuit which consumes 13.5W power at a supply voltage level of V_{dd}=1.5V

Parameter	Value
V_0	4V
η	0.9
K/T	1.7
α	1.5
V_{th}	0.6V
$mC_{sw}/(2CAP_0)$	Normalized to 1

BD-D Product Curves for Different β `s (fixed latency)



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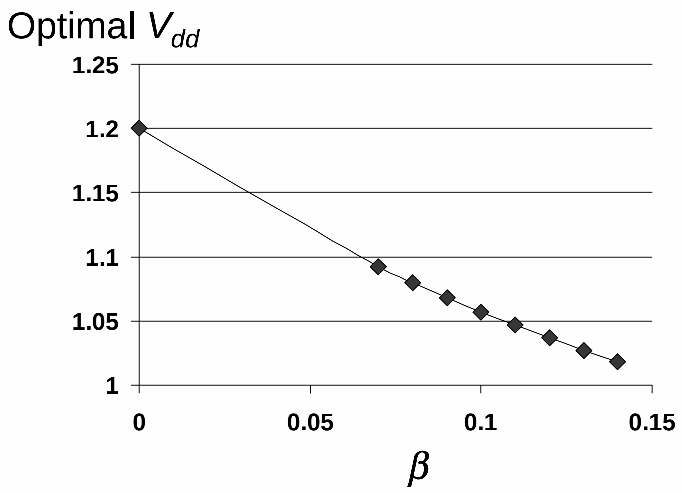
Optimal V_{dd} for Minimum BD-D Product (fixed latency)



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Case 2: Variable Operation Latency

Assume *T* is proportional to the circuit delay:

$$T \propto t_d \Rightarrow T = m' \frac{V_{dd}}{(V_{dd} - V_{th})^{\alpha}}, \qquad 1 < a \le 2$$

The *BD-D* product becomes:

$$BD\text{-}D = \frac{m \cdot C_{sw}}{2 \cdot CAP_0} \cdot \frac{V_{dd}^3}{(1 - \beta \cdot k \cdot V_{dd} \cdot (V_{dd} - V_{th})^{\alpha} / m') \cdot (V_{dd} - V_{th})^{\alpha}}$$

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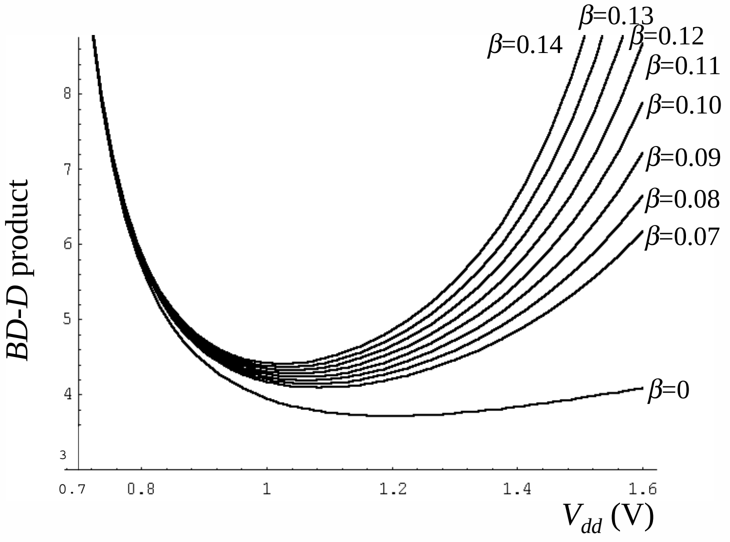
Analysis Setups

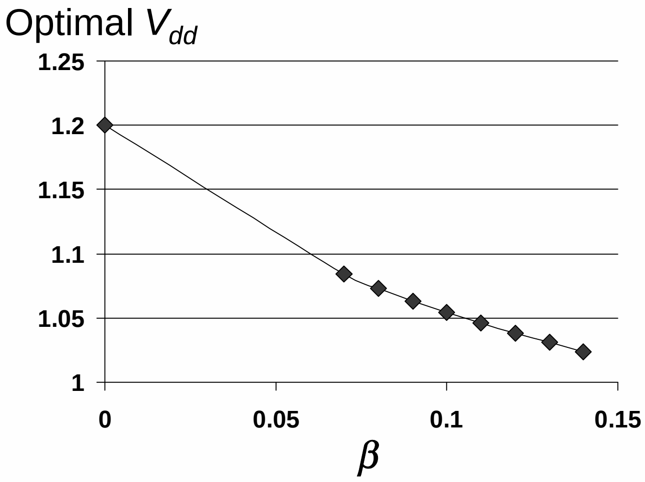
Consider a VLSI circuit which consumes 13.5W power at a supply voltage level of V_{dd}=1.5V

Parameter	Value
V_0	4V
η	0.9
K/m'	3.0
α	1.5
V_{th}	0.6V
$mC_{sw}/(2CAP_0)$	Normalized to 1

BD-D Product Curves for Different β `s (variable latency)



Optimal V_{dd} for Minimum BD-D Product (fixed latency)



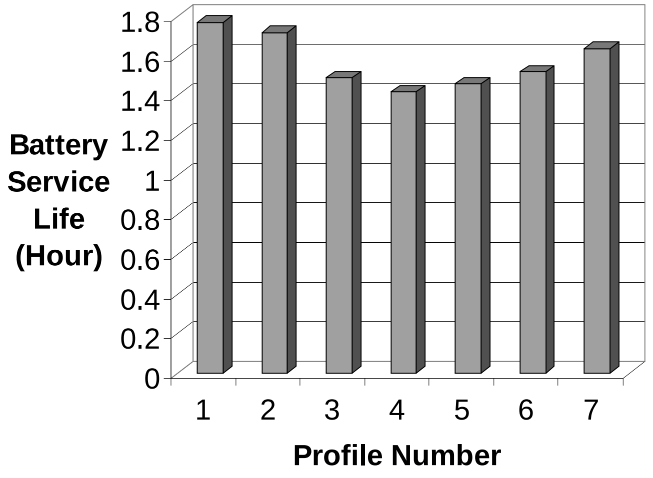
Observation III

When using an integrated battery-hardware model, the optimal supply voltage (i.e. one that minimizes the Battery Discharge - Delay Product) is lower than the ideal case.

Battery-Circuit Simulation Setup

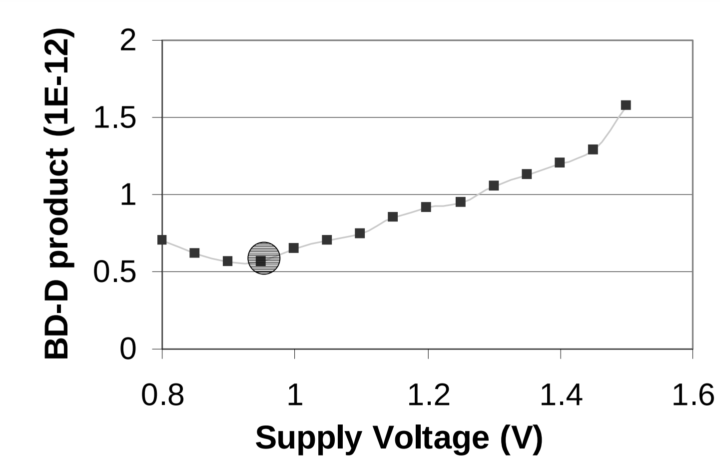
- An HSPICE macro-model is used for the battery source
- Battery characteristics are obtained from the data sheets of a commercial Lithium battery manufacturer
- Efficiency of the DC/DC converter is set to 90%
- Seven different current profiles with the same mean value are used for the first part (profile-dependent BSL):
  - (1) δ-function with mean of 1.5A
  - (2) Normal distribution with σ=0.1
  - (3) Normal distribution with σ=0.5
  - (4) Uniform distribution over region [0, 3]
  - (5) Bi-modal δ-function with means at 0.25A and 2.75A
  - (6) Bi-modal δ-function with means at 0.5A and 2.5A
  - (7) Bi-modal δ-function with means at 1A and 2A
- A 0.35μ CMOS process technology (BSIM3 models) is used for the second part (BD-D product)

HSPICE Simulation Results: the BSL



USC
Low Power
CAD

HSPICE Simulation Results: the BD-D Product



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Pedram

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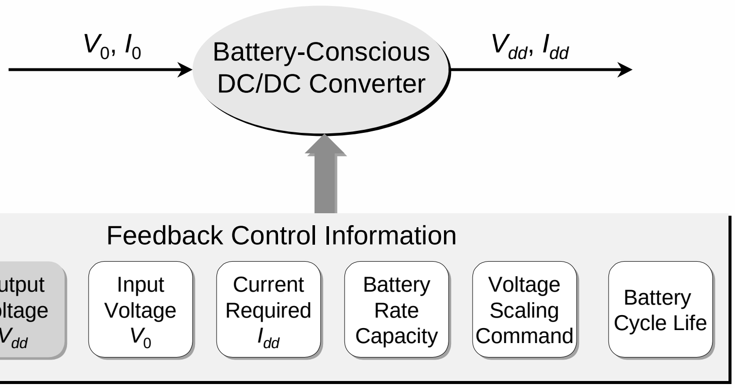
Implications for Low Power Design

- ❑ Current profile has a significant impact on the battery service life
  - Must reduce the variance of the average current over some time interval (e.g. in the order of mS)
  - Possible methodologies are balanced task scheduling, dynamic voltage scaling, etc.
- ❑ When considering the battery characteristics, the optimal supply voltage is lower than initially thought
  - Achieving higher circuit performance by increasing the supply voltage level is more costly than previously thought

Massoud
Pedram

Future Work:
Battery-Conscious DC/DC Converter



V_0, I_0

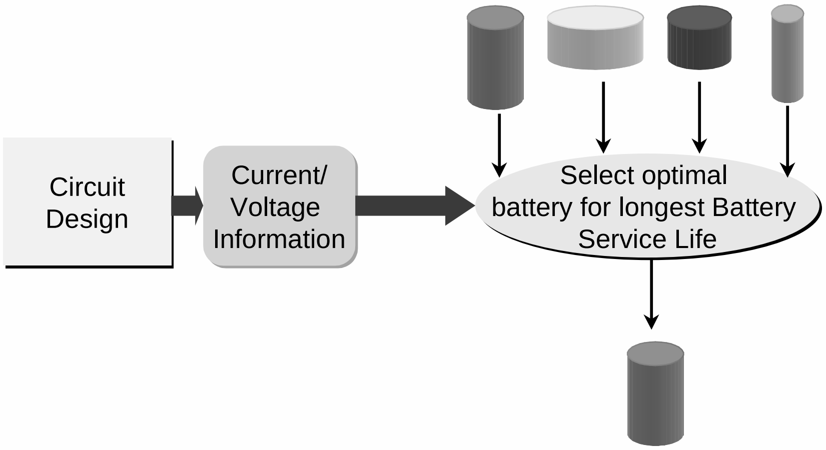
Battery-Conscious DC/DC Converter

V_{dd}, I_{dd}

Feedback Control Information

- Output Voltage V_{dd}
- Input Voltage V_0
- Current Required I_{dd}
- Battery Rate Capacity
- Voltage Scaling Command
- Battery Cycle Life

Optimal Battery Selection

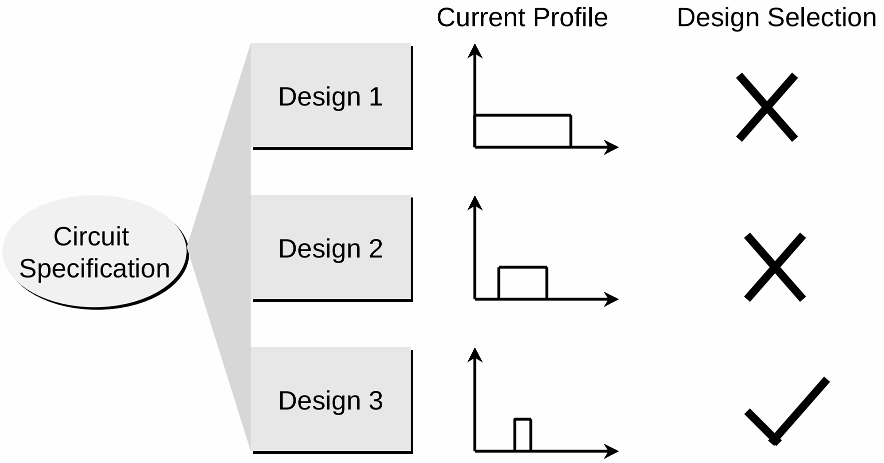


Circuit Design

Current/ Voltage Information

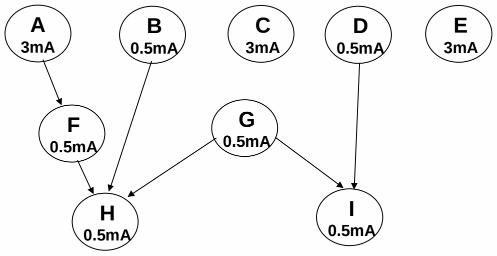
Select optimal battery for longest Battery Service Life

Design Optimization for Longer Battery Service Life



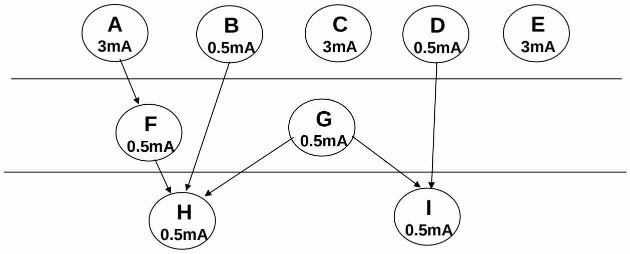
Task Scheduling for Maximum Battery Life

- Different task scheduling leads to different current profile
- Balanced average current scheduling results in maximum battery life
- Scheduling in task-level (in order of ms)
- Example A:
  - Each task takes the same amount of time to compute but different average current

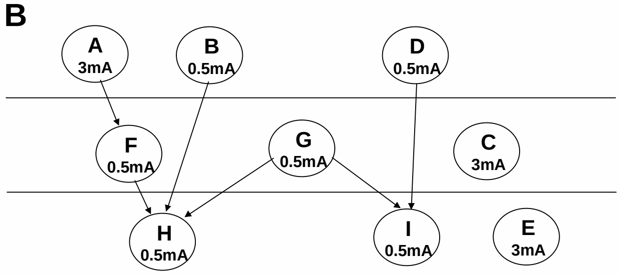


Effect of Different Task Schedules

Schedule A

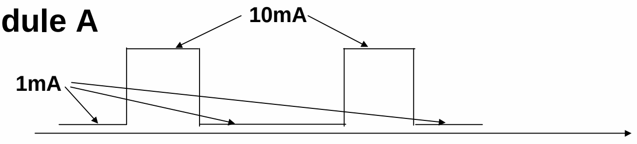


Schedule B

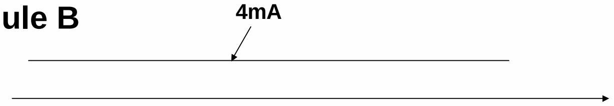


Current Profile of Different Task Schedules

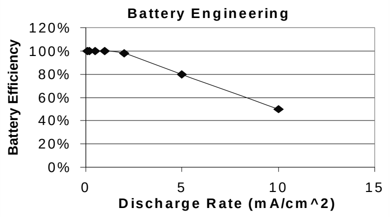
Schedule A



Schedule B



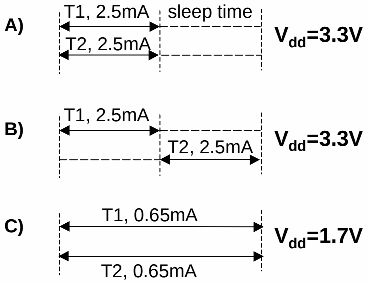
Using the battery characteristic of battery engineering



Schedule	Normalized Battery Life
A	1.00
B	1.56

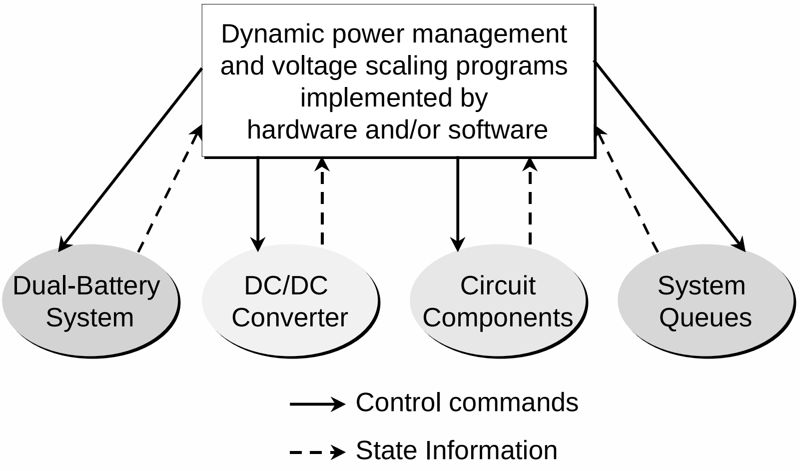
Voltage Scaling and Power Management

- ☐ Traditional system-level power management which maximizes the system sleep time may not be optimal for maximum the battery life because of the variation of current profile
- ☐ Coupling with task-level dynamic voltage scaling can further optimize the battery life
- ☐ An example



Schedule	Normalized Battery Life
A	1.00
B	1.21
C	2.40

Dynamic Power Management and Voltage Scaling


Dynamic power management and voltage scaling programs implemented by hardware and/or software

Conclusions

- It is essential to build an integrated battery-hardware model for the battery-powered micro-electronic circuits and systems
- Low power optimization decisions must be guided by a new design metric, I.e., the battery discharge rate -delay product
- Fusion of battery engineering technology and low power CMOS design technology is a must
- Methodologies and techniques for power-aware design of battery-operated computing and communication devices must be altered to account for the electro-chemical and output characteristics of real battery cells that power such devices
- Battery-conscious DC-DC converter design, battery-aware low power CMOS design, application-specific battery cell selection, dual battery systems, dynamic power management at the system-level are a few of the important problems that must be addressed