Recent Results of the Current Source Model-Based Approach for Timing Analysis

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SRC LPD Review

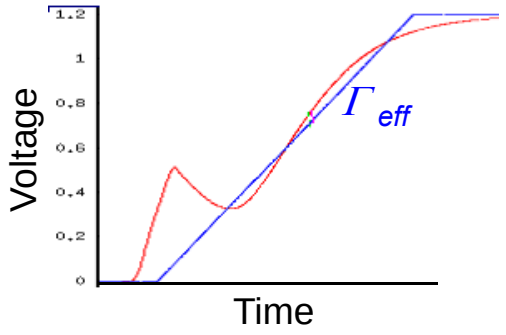
Oct 17, 2007

Outline

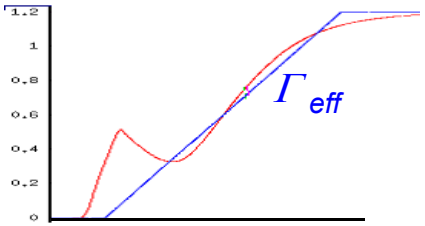
- Background
- Current Source Modeling (CSM) for Logic Cell Delay Analysis Under Noisy Input Waveforms
- A Current-based Method for Short Circuit Power Calculation (CSPC) Under Noisy Input Waveforms
- A Current Source Model for CMOS Sequential Cells
- Conclusion

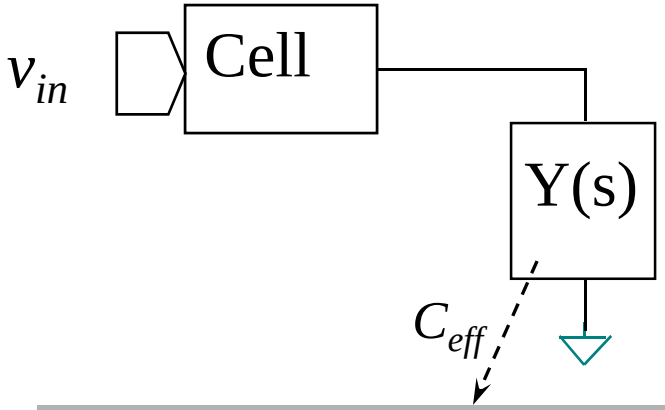
Introduction

- Scaling and noise
  - The down scaling of layout geometries:
    - Aggravation of noise effects, such as the capacitive crosstalk noise
- Logic cell delay techniques
  - Single reference point (arrival time)
  - Rise/fall slope (transition time)
- Conventional logic cell delay techniques are inaccurate:
  - Approximation of input with a saturated ramp, i.e., Γ_{eff}



Conventional Pre-Characterization

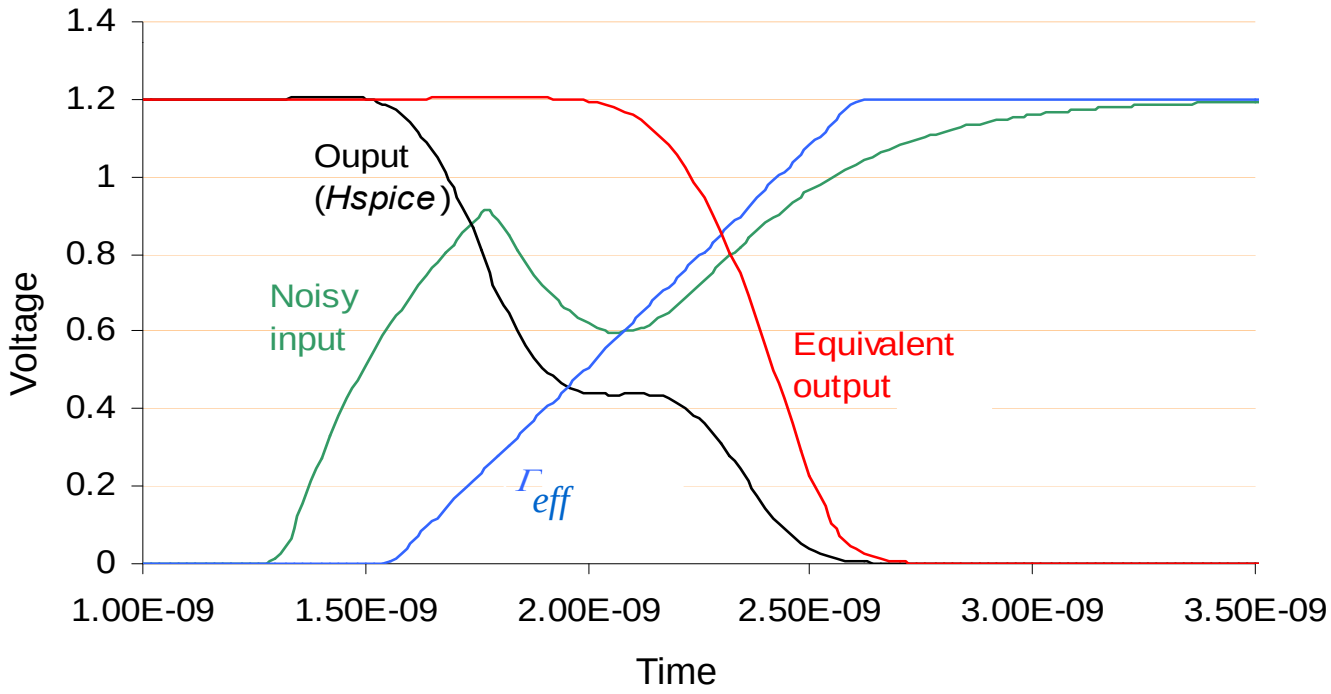




	C_{eff}^{1}	C_{eff}^{2}	…	C_{eff}^{i}	…	C_{eff}^{N}
Tr_{in}^{1}						
Tr_{in}^{2}						
⋮						
Tr_{in}^{j}				$Tr_{out}(i,j)$, $delay(i,j)$		
⋮						
Tr_{in}^{M}						

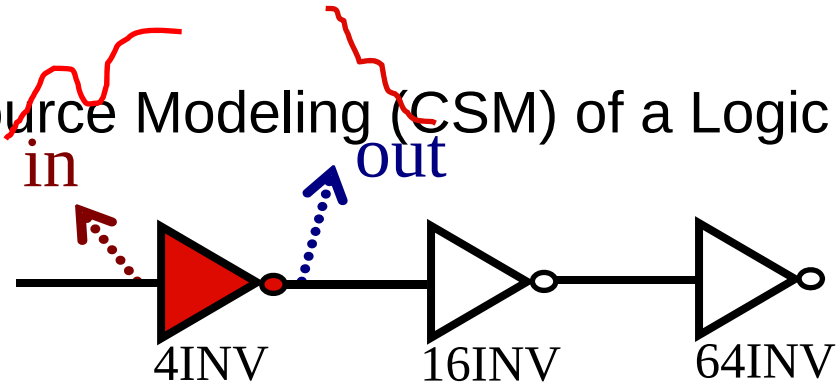
Logic Cell Timing Analysis Issues

- Conventional logic cell delay techniques ignore the actual shape of the waveform
  - Pessimism in approximation with a saturated ramp



Logic Cell Delay Modeling

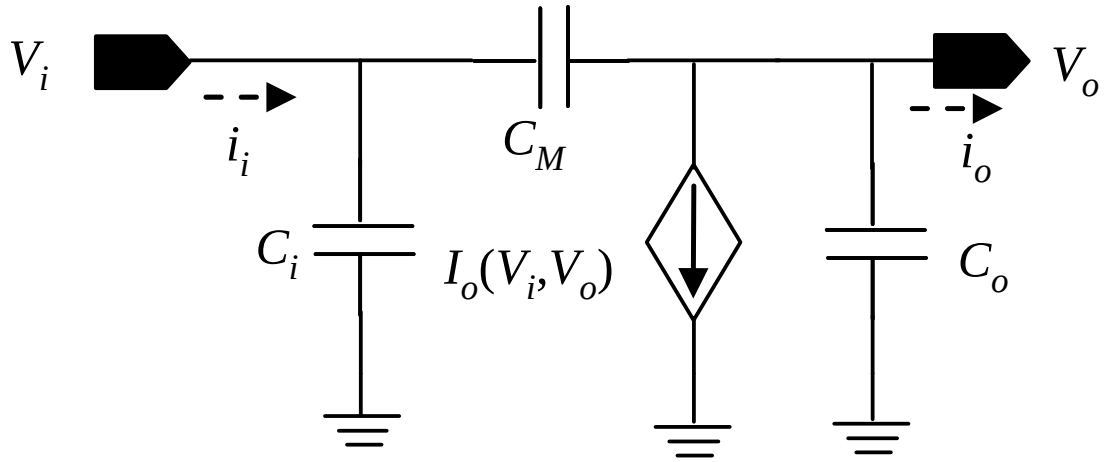
- Accurate Logic Cell Timing Analysis:
  - Consider the actual shape of the input waveform
- Problem Statement:
  - Given: A (noisy) input voltage waveform
  - Objective: Determine the output voltage waveform
    - Minimum error w.r.t. the **actual shape** of the output waveform
- Construct the output based on the input voltage and the logic cell model
- Solution:
  - Current Source Modeling (CSM) of a Logic Cell



Current Source Modeling

- Some applications
  - Path-based timing analysis inside a signoff tool:
    1. Identification of a set of critical paths by performing conventional static timing analysis (STA)
    2. Accurate timing and noise analysis on the target path by using the CSM model
  - Noise analysis to determine the delay and slew changes
    - Used inside the STA tools as part of the signal integrity analysis (example: PrimeTime Signal Integrity, PTSI)
  - Simulation engine for waveform propagation

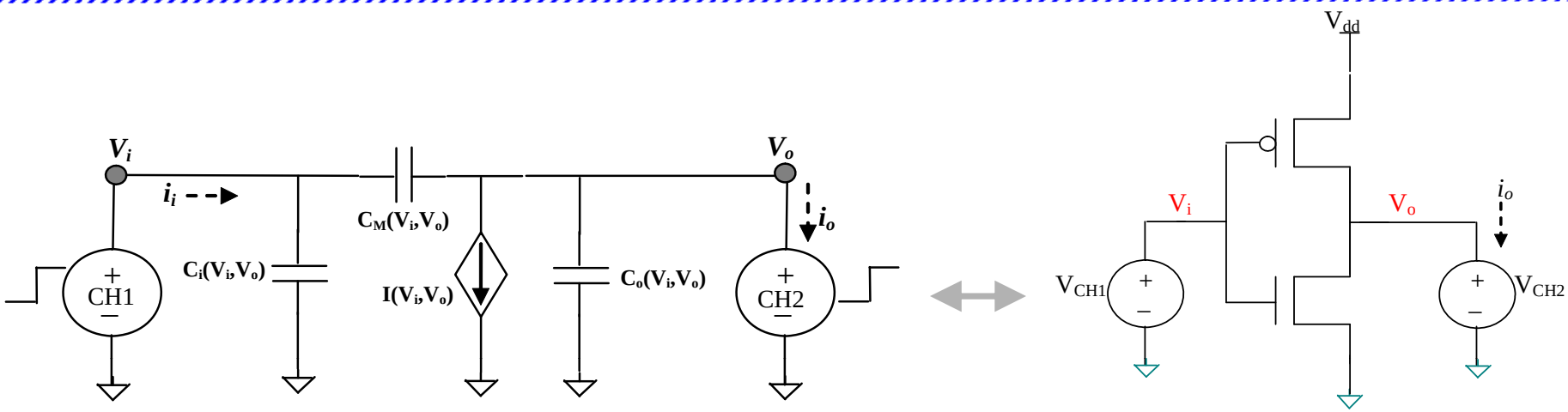
Our Current Source Model (DAC 06)



$$i_o + C_o \frac{\Delta V_o}{\Delta t} + I(V_i, V_o) + C_M \frac{\Delta V_o}{\Delta t} - C_M \frac{\Delta V_i}{\Delta t} = 0$$

- The non-linear behavior of the logic cell:
  - 2-D lookup table to store $I(V_i, V_o)$
- Parasitic effects in the logic cell:
  - 2-D lookup tables to store $C_i(V_i, V_o)$, $C_M(V_i, V_o)$, and $C_o(V_i, V_o)$
- Series of SPICE simulations to pre-characterize various elements of the CSM model

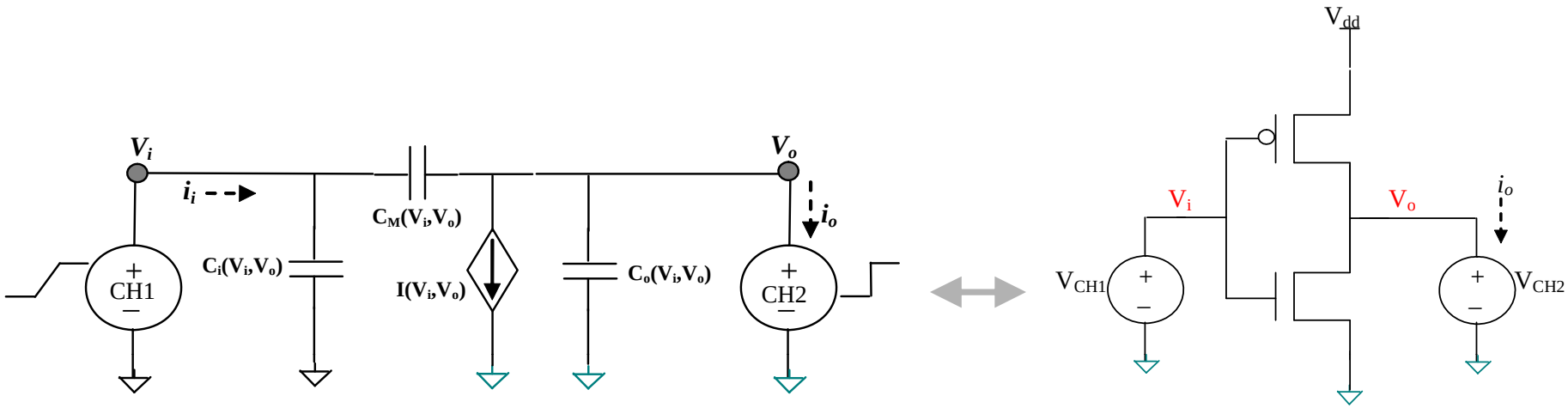
Pre-characterization: Current Source



$$i_o + C_o\frac{\Delta V_o}{\Delta t} + I(V_i,V_o) + C_M\frac{\Delta V_o}{\Delta t} - C_M\frac{\Delta V_i}{\Delta t} = 0$$

- $I(V_i,V_o)$:
  - Apply DC voltage sources V_{CH1} and V_{CH2} to the input and output
  - Measure i_o (the current going trough V_{CH2}) in SPICE and fill the entry $I(V_{CH1},V_{CH2})$ of the table
  - Sweep the DC voltage sources

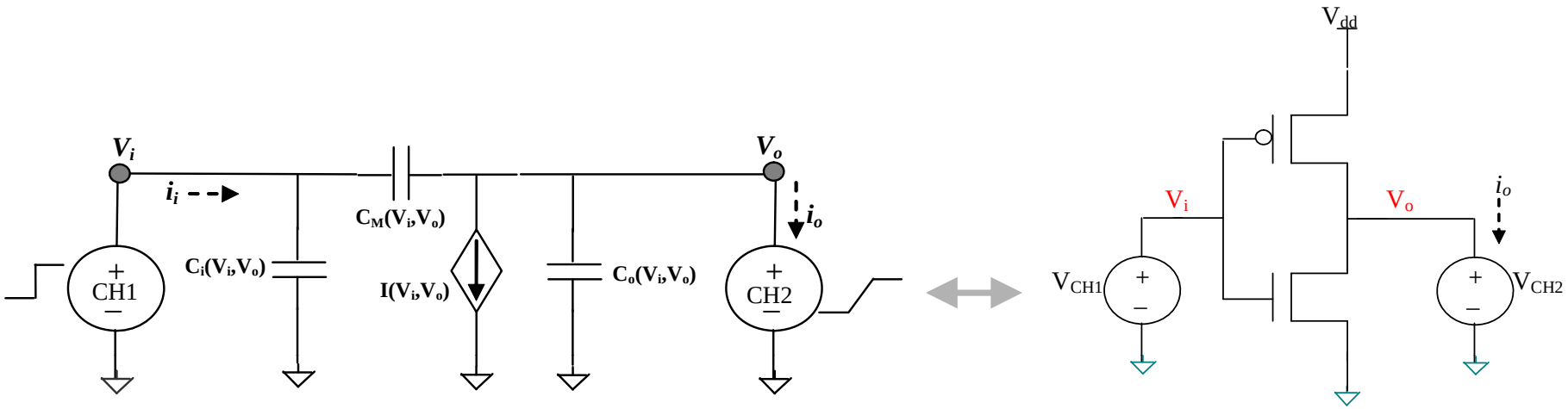
Pre-characterization: Parasitics (C_M)



$$i_o + C_o \frac{\Delta V_o}{\Delta t} + I(V_i, V_o) + C_M \frac{\Delta V_o}{\Delta t} - C_M \frac{\Delta V_i}{\Delta t} = 0$$

- $C_M(V_i, V_o)$
  - Apply a ramp voltage source to input and a DC source to output
  - Measure i_o in SPICE for different voltage values at the input
  - Calculate C_M from the KCL eqn and fill out one column of the table
  - Sweep the DC voltage source at the output

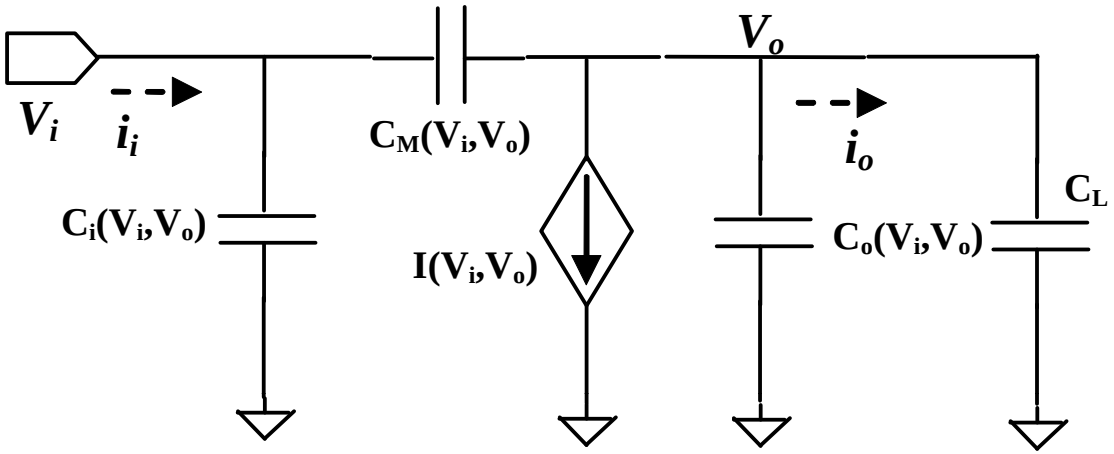
CSM Pre-characterization: Parasitics (C_o)



$$i_o + C_o \frac{\Delta V_o}{\Delta t} + I(V_i, V_o) + C_M \frac{\Delta V_o}{\Delta t} - C_M \frac{\Delta V_i}{\Delta t} = 0$$

- $C_o(V_i, V_o)$
  - Apply a DC source to input and a ramp voltage source to output
  - Measure i_o in SPICE for different voltage values at the output
  - Calculate C_o from the KCL eqn and fill out one row of the table
  - Sweep the DC voltage source at the input

Voltage Calculation Using CSM

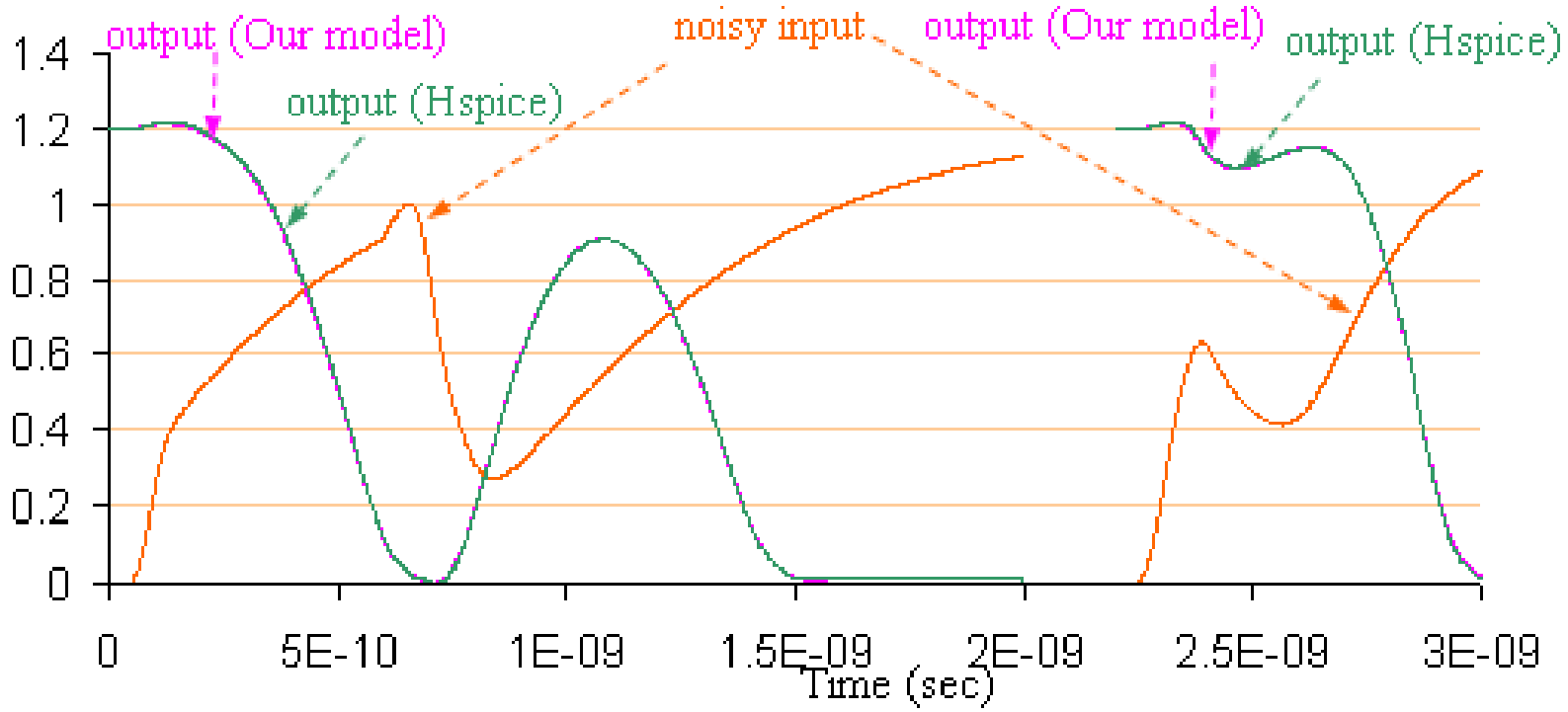


$$C_L \frac{\Delta V_o}{\Delta t} + C_o \frac{\Delta V_o}{\Delta t} + I(V_i, V_o) + C_M \frac{\Delta V_o}{\Delta t} - C_M \frac{\Delta V_i}{\Delta t} = 0$$

$V_o(t_{k+1})$: Calculated based on $V_o(t_k)$ and $V_i(t_k)$, $V_i(t_{k+1})$ and the current source and parasitic capacitance values

$$V_o(t_{k+1}) = V_o(t_k) + \frac{1}{C_L + C_o + C_M} \cdot \left\{ C_M \cdot \left(V_i(t_{k+1}) - V_i(t_k) \right) - I\left(V_i(t_{k+1}), V_o(t_k) \right) \cdot \Delta t \right\}$$

Experimental Results



- HSPICE and our CSM-based results for some crosstalk-induced noisy waveforms
- Logic cell: Minimum sized inverter in 130nm library

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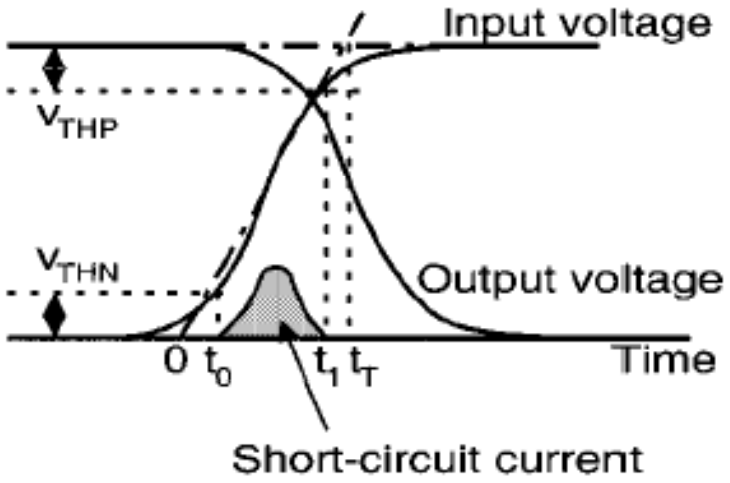
Short Circuit Power Calculation



- Short circuit current:
  - Flows from the Vdd rail to ground during an output transition
  - Depends on the duration of time that transistors in the pull-up and pull-down sections of a CMOS logic cell operate in each region of the transistor operation
  - Depends on both input and output voltage waveforms
- How to measure short circuit current and energy dissipation?

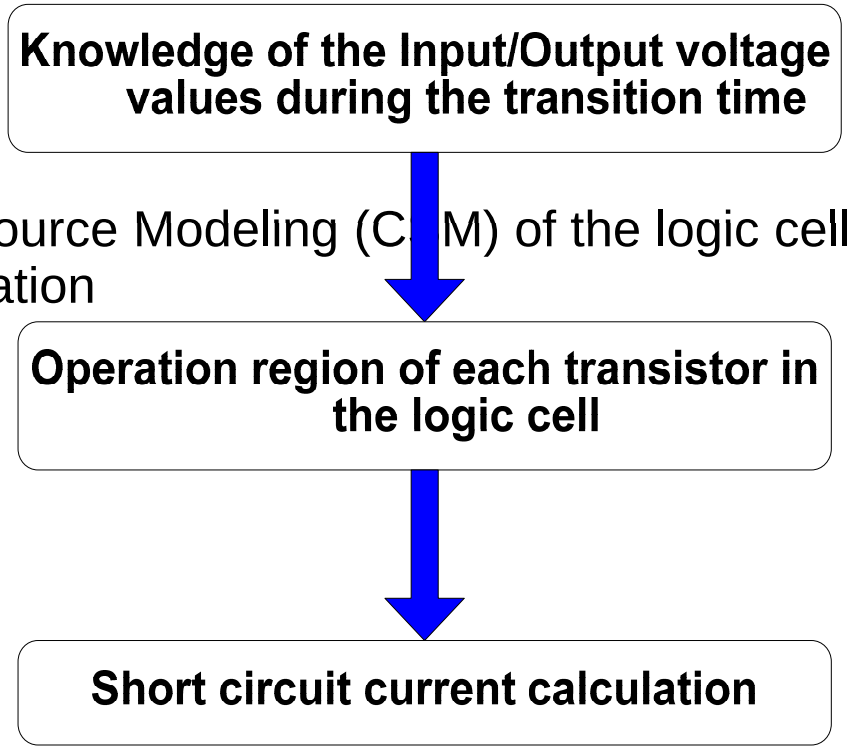
Short Circuit Power Calculation Flow

- Problem statement:

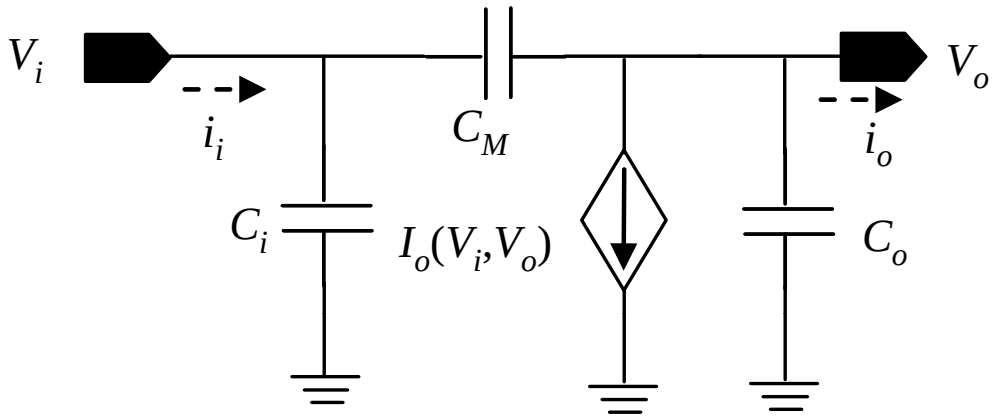
  Develop a short circuit power calculator capable of handling noisy inputs (including glitches) with arbitrary shapes

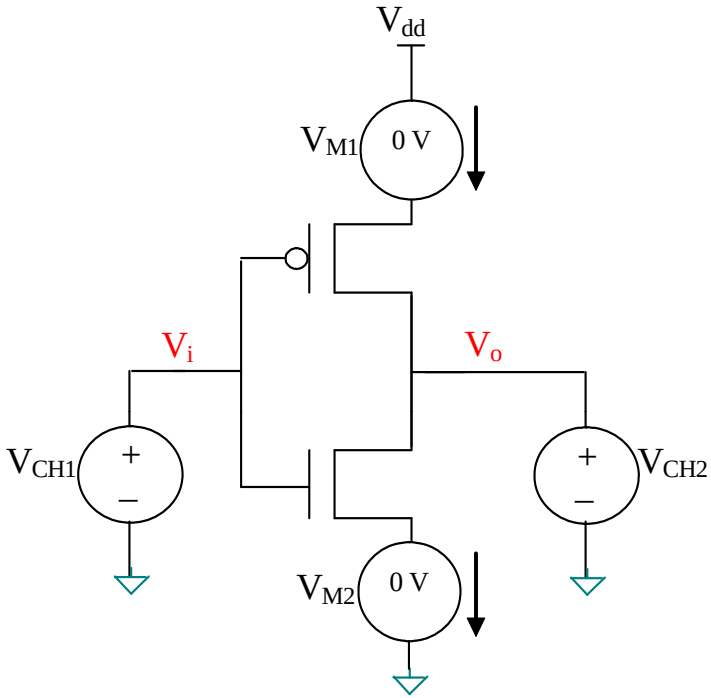
- Solution:

  Utilize Current-Source Modeling (CSM) of the logic cells for the purpose of SC power calculation



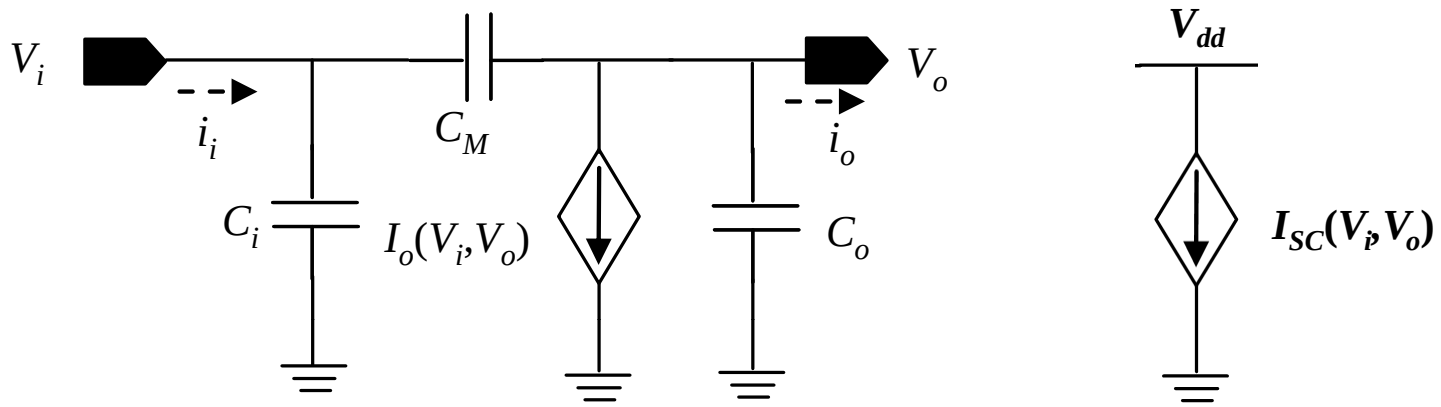
Short Circuit Current Pre-characterization





- $I_{sc}(V_{CH1},V_{CH2}) = I(V_{M1}) \cap I(V_{M2})$
- A new 2-D lookup table is created to store the $I_{sc}(V_{CH1},V_{CH2})$ values
- Complexity of the CSM does not increase by the SCC pre-characterization

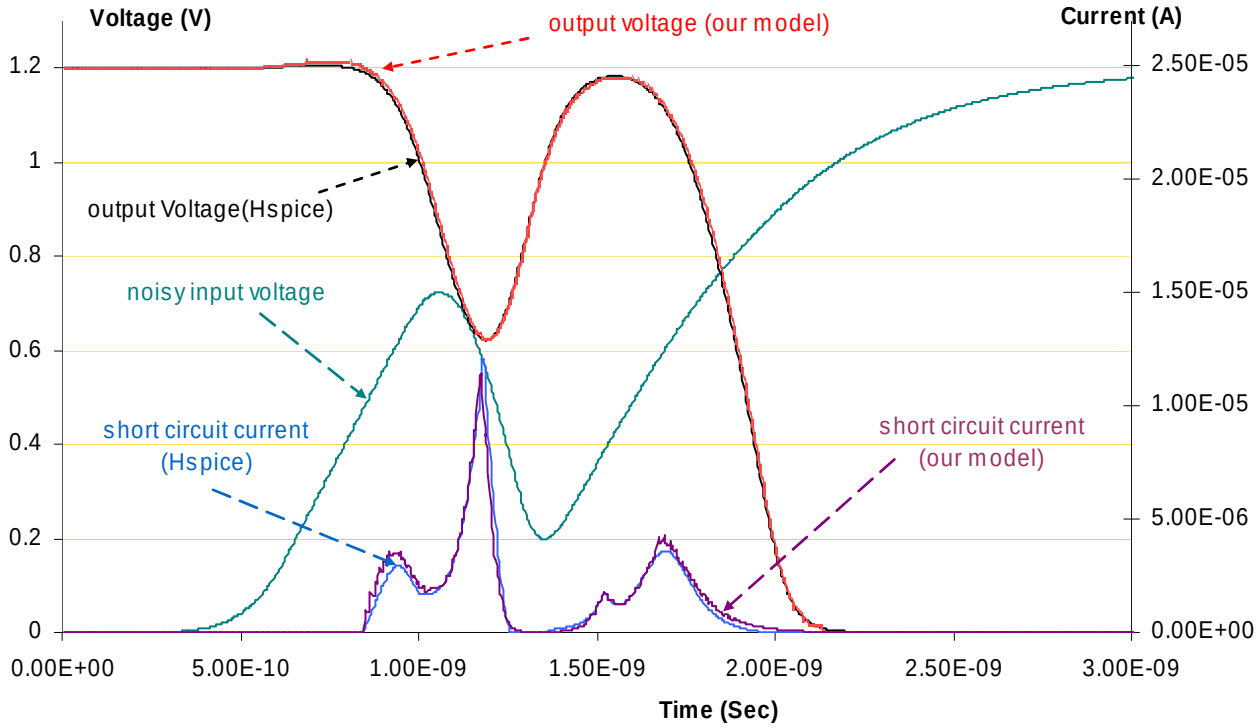
CSM-based Short Circuit Power Calculator (CSPC)



- Step 1: Construct the output voltage waveform based on the noisy input waveform by using our CSM-based calculator
- Step 2: At each time instance, read the corresponding short circuit current from the look up table and thereby construct the exact short circuit (SC) current waveform
- Step 3: Report the short circuit energy dissipation associated with the input-output transition as the area under the SC current waveform times V_{DD}

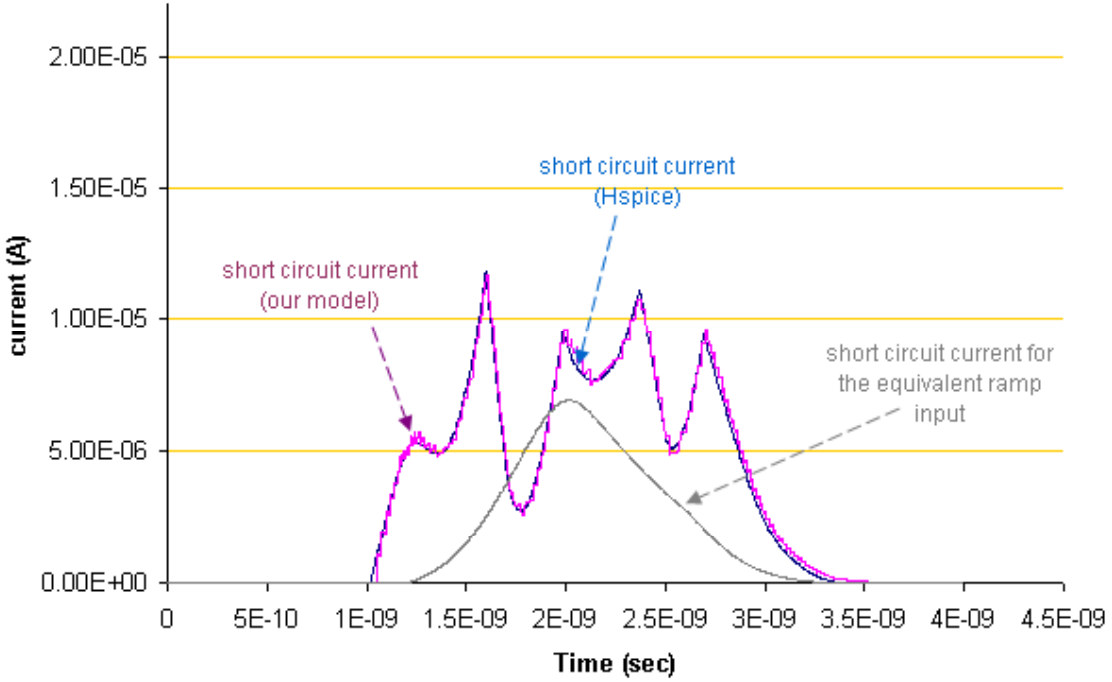
Experimental Results – Accuracy of CSPC

- Noisy waveform given to a minimum sized inverter with a FO4 loading in our 130nm cell library
- Switching energy consumption per transition is 8.89fJ
- The SC energy dissipation is 2.68fJ (2.78fJ) per Hspice (CSPC)
- E_{sc}/E_{sw} ratio of 30.1%



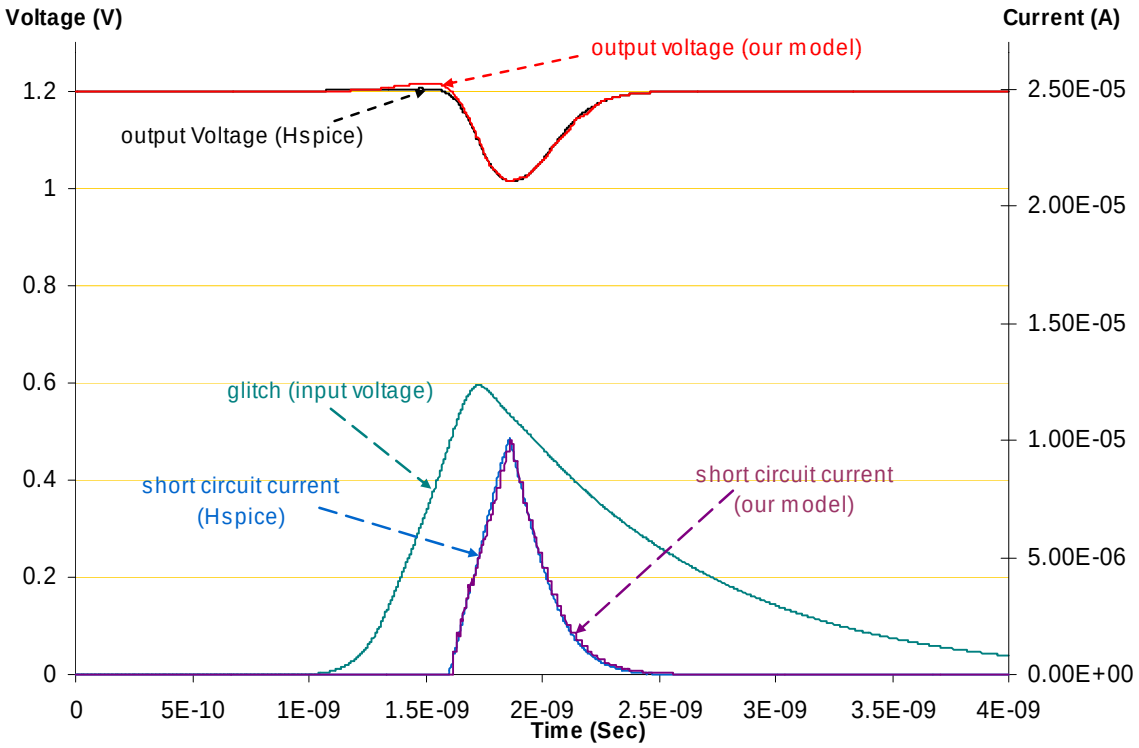
Comparison with Previous Techniques

- Saturated ramp approximation of input waveform and use of pre-characterized lookup tables $E_{sc}(t_{in},C_L)$
  - SC energy dissipation reported by ramp approximation is 7.1fJ
  - 45.9% error w.r.t. to Hspice short circuit energy report of 15.45fJ
  - SC energy dissipation reported by CSPC is 15.61J (1% error)
  - Shape of the input waveform should not be ignored

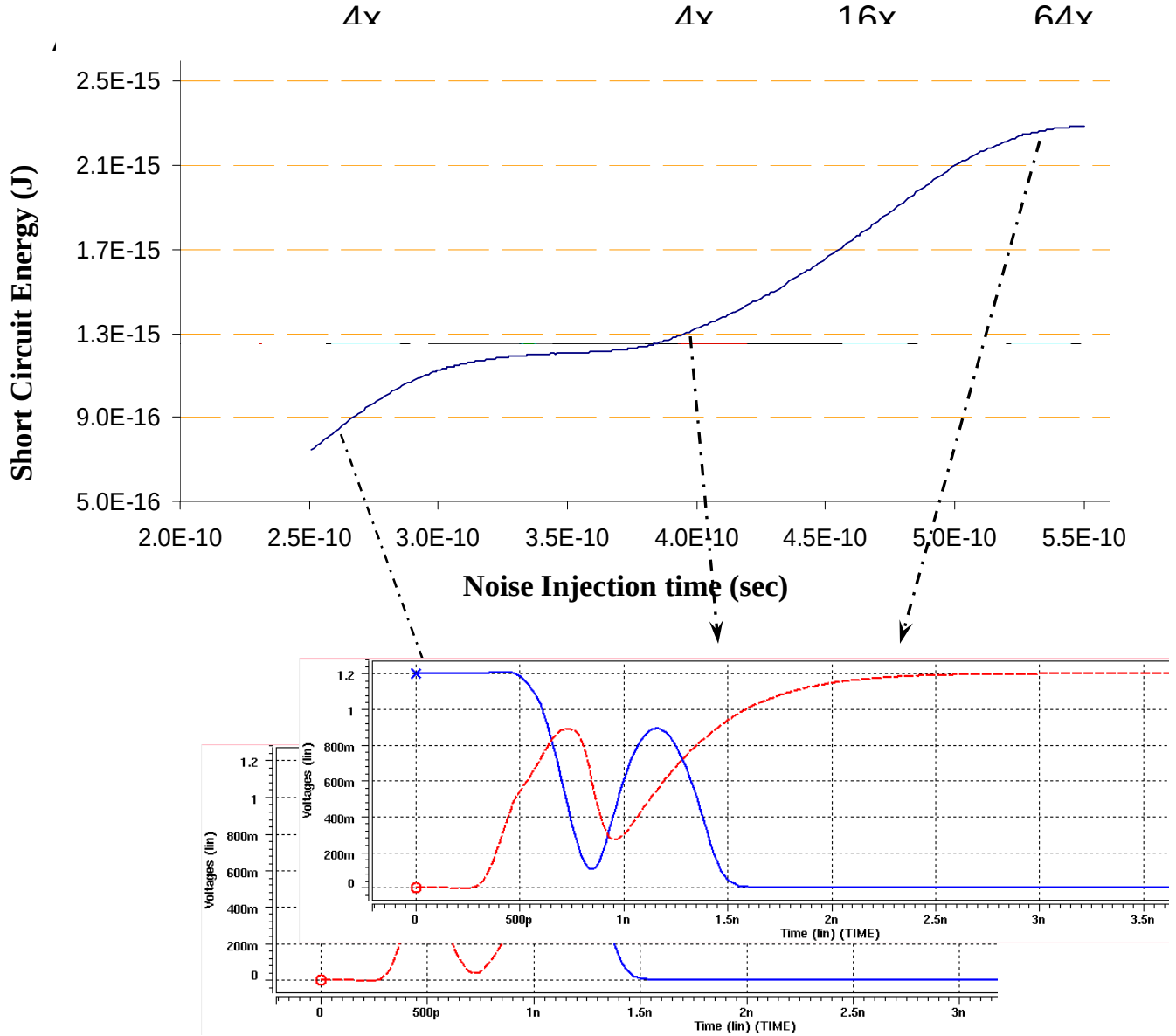


Experimental Results – Glitches

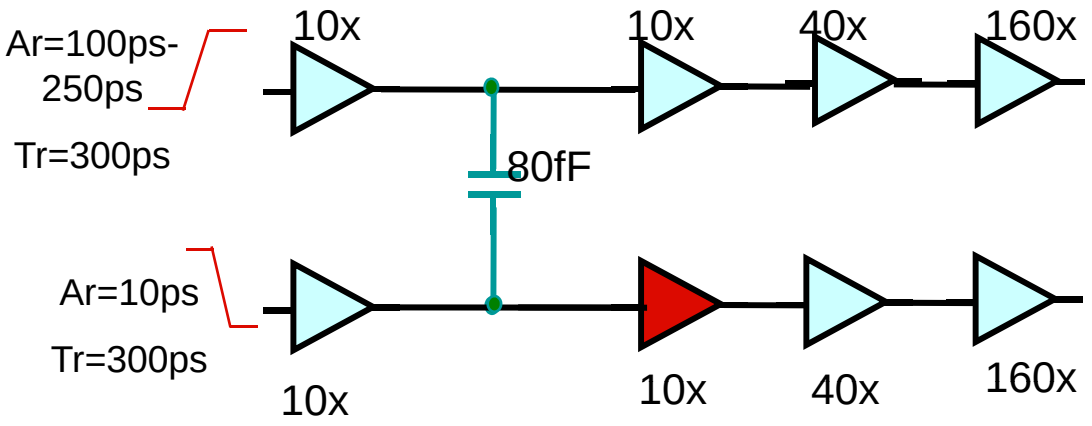
- Glitches are typically ignored by the timing analysis or a validation tools
  - The resulting SC energy dissipation may not be negligible (3.5fJ for the example shown below)

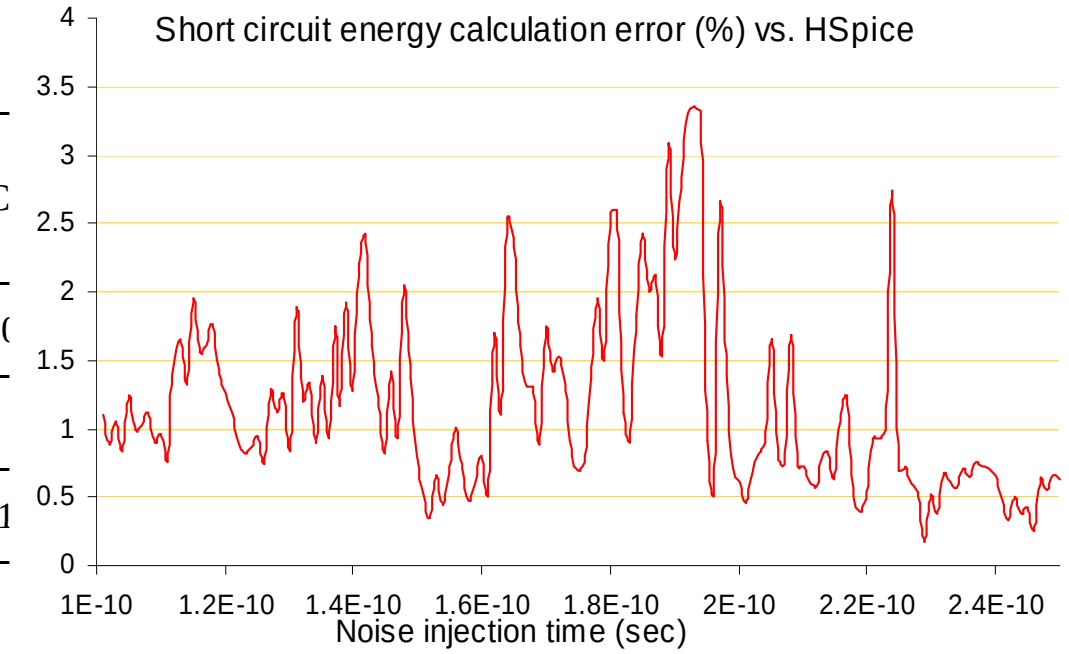


Short Circuit Energy in the Presence of Crosstalk



Accuracy and Runtime of CSPC





Logic C		ime dup
INV 1(		40
NAND2		20
AOI21 1		50

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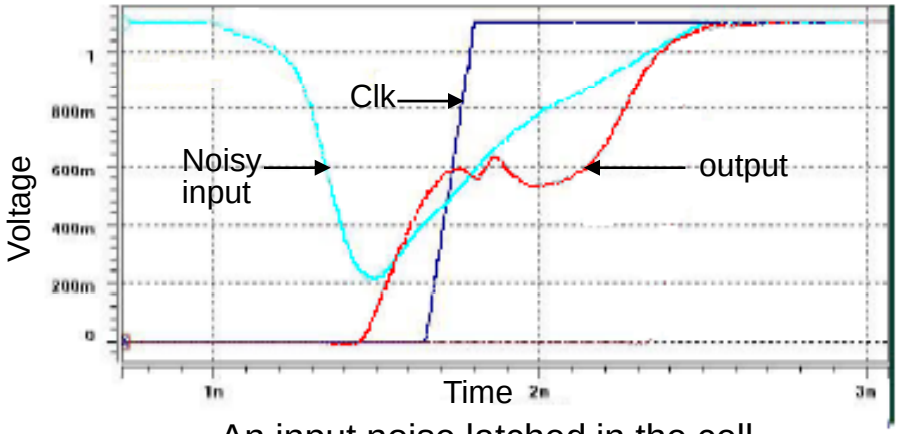
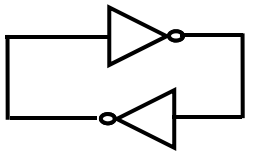
Noise and sequential cells

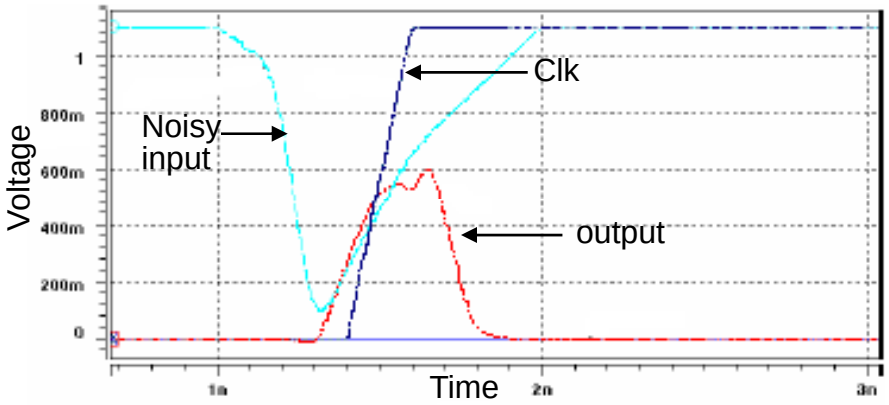
- Does the noisy input cause a functional error in the circuit?



An input noise latched in the cell



Feedback loop in latches

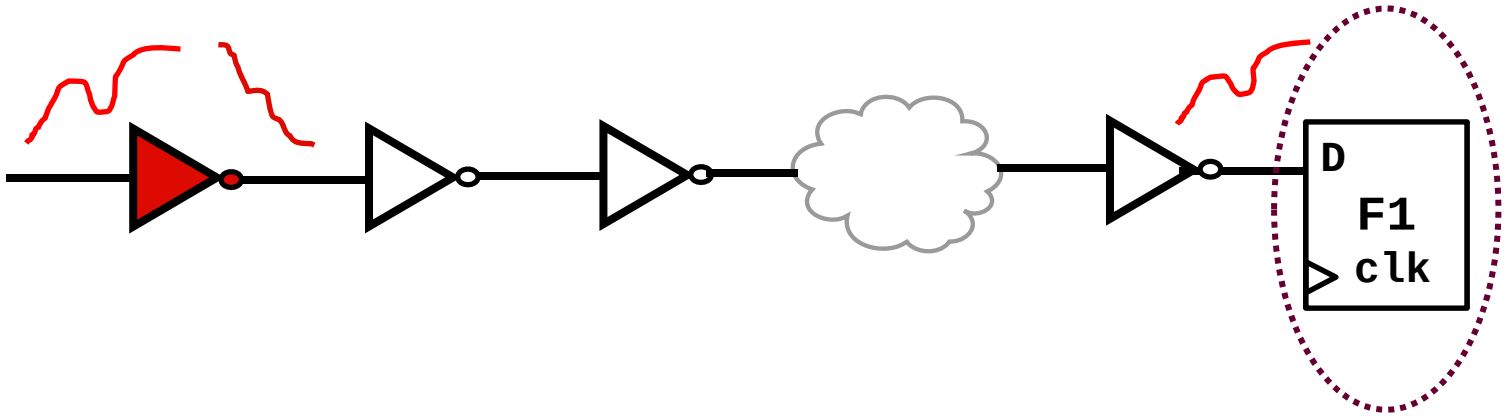


An input noise not latched in the cell

N. Oh, L. Ding and A. Kasnavi “Fast Sequential Cell Noise Immunity Characterization Using Meta-stable Point of Feedback Loop” ISQED’06

CSM for Sequential Cells

- Output waveform of the sequential cell is important for calculating the next stage timing information
- A complete CSM-based solution for performing the delay and noise analysis on a set of selected paths is needed



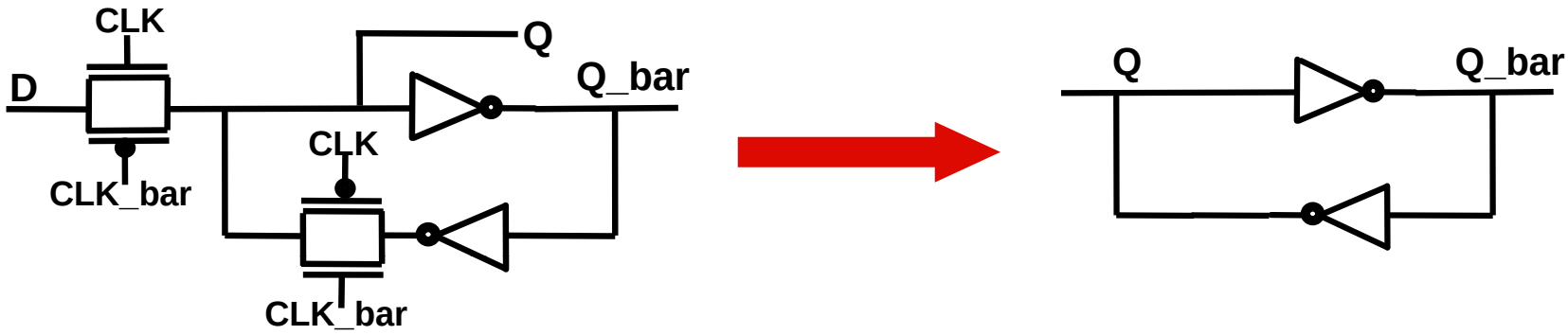
- We must develop CSM models of sequential cells

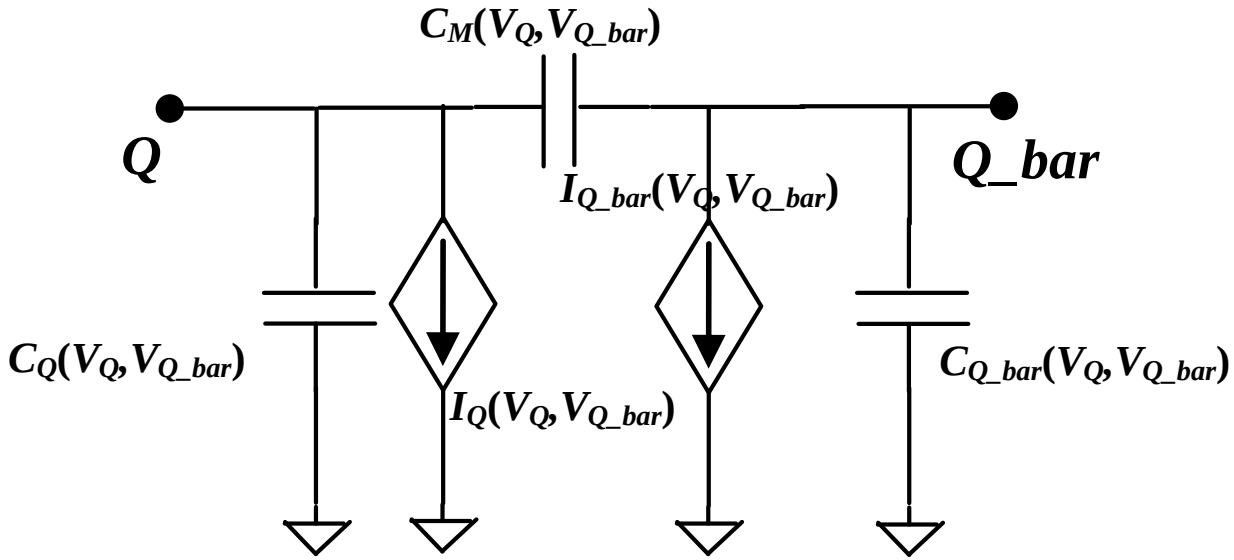
Current Source Modeling of Latch

- At each time latch is in one of the following modes:
  - Steady state transparent mode (CLK=1)
  - Transition mode (switching CLK)
  - Steady state hold (opaque) mode (CLK=0)
- CSM for latch which handles all three modes automatically:

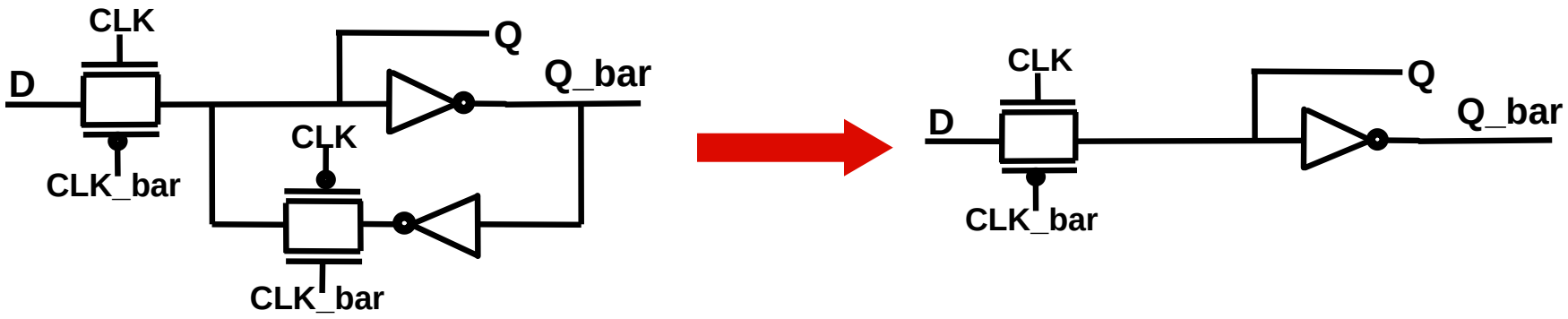
Steady-State Feedback Mode (CLK=0)

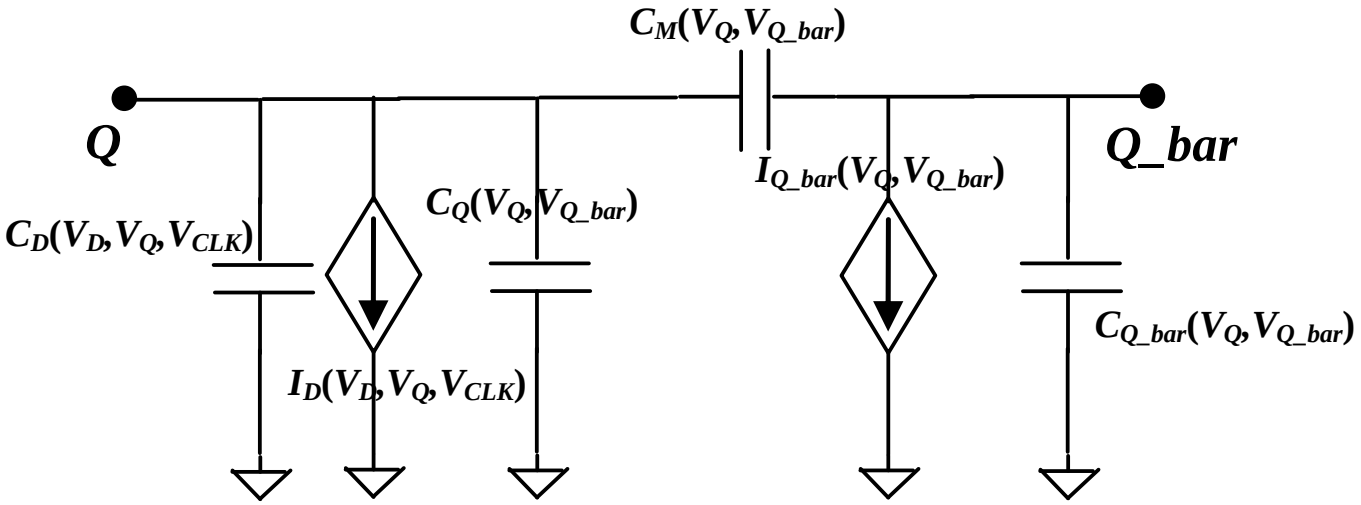
- Modeling the feedback loops:



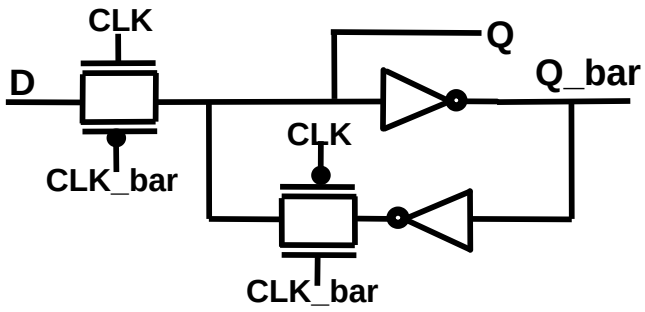


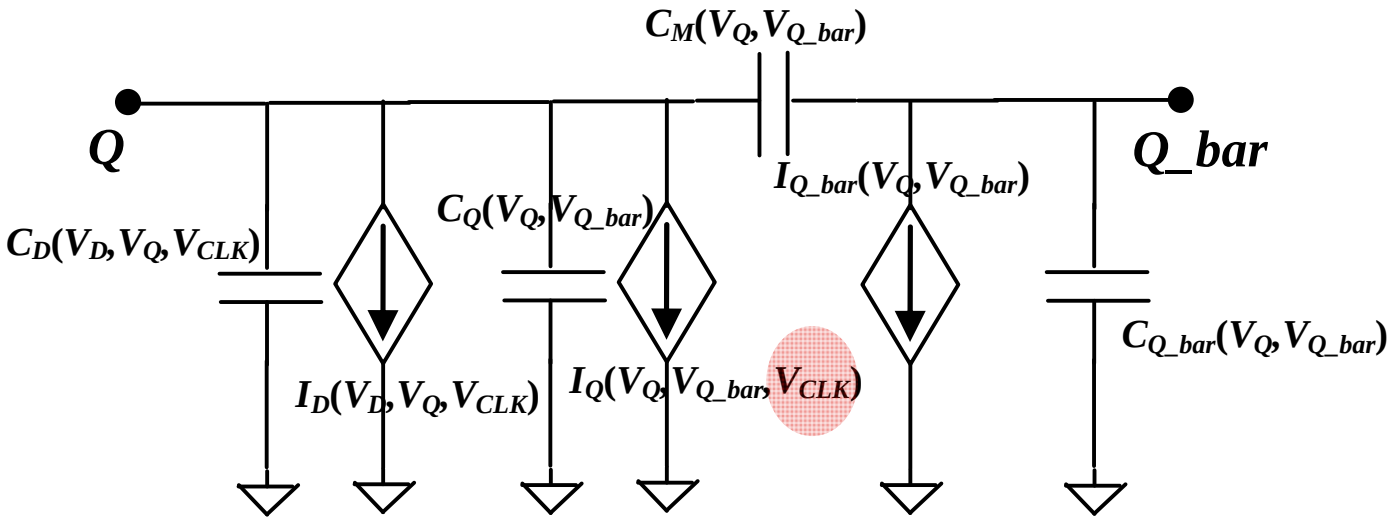
Steady-State Transparent Mode (CLK=1)





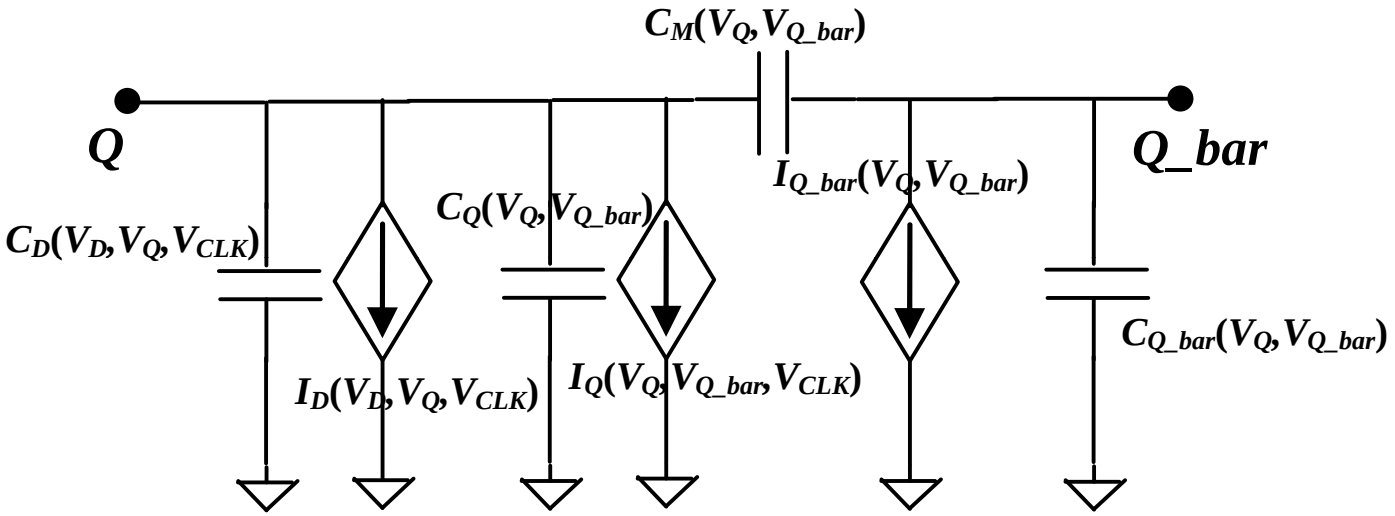
Transition Mode (Switching CLK)





Voltage Calculation

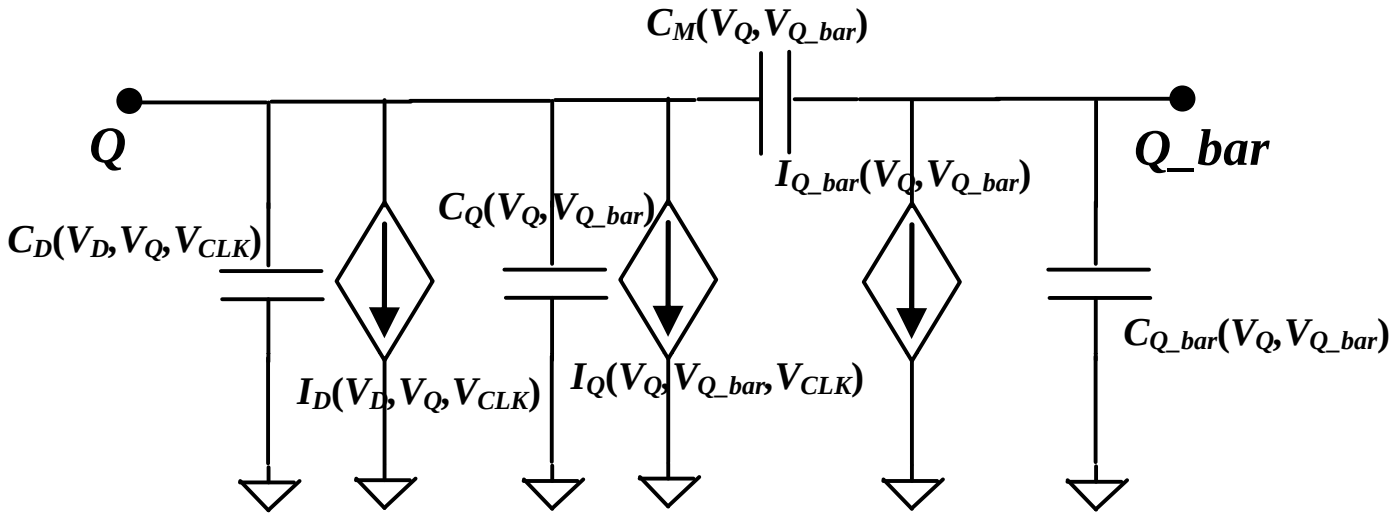
- CSM automatically adapts itself to different modes



Computing $V_Q(t_{k+1})$:

$$V_Q(t_{k+1}) - V_Q(t_k) = \frac{\left\{ I_D\left(V_D(t_{k+1}), V_Q(t_k), V_{CLK}(t_{k+1})\right)\cdot\Delta t + I_Q\left(V_Q(t_k), V_{Q\_bar}(t_k), V_{CLK}(t_{k+1})\right)\cdot\Delta t \right.}{\left. + C_M\left(V_Q, V_{Q\_bar}\right)\cdot\left(V_{Q\_bar}(t_k) - V_{Q\_bar}(t_{k-1})\right)\right\}}$$
$$C_Q\left(V_Q, V_{Q\_bar}\right) + C_M\left(V_Q, V_{Q\_bar}\right) + C_D\left(V_D, V_Q, V_{CLK}\right)$$

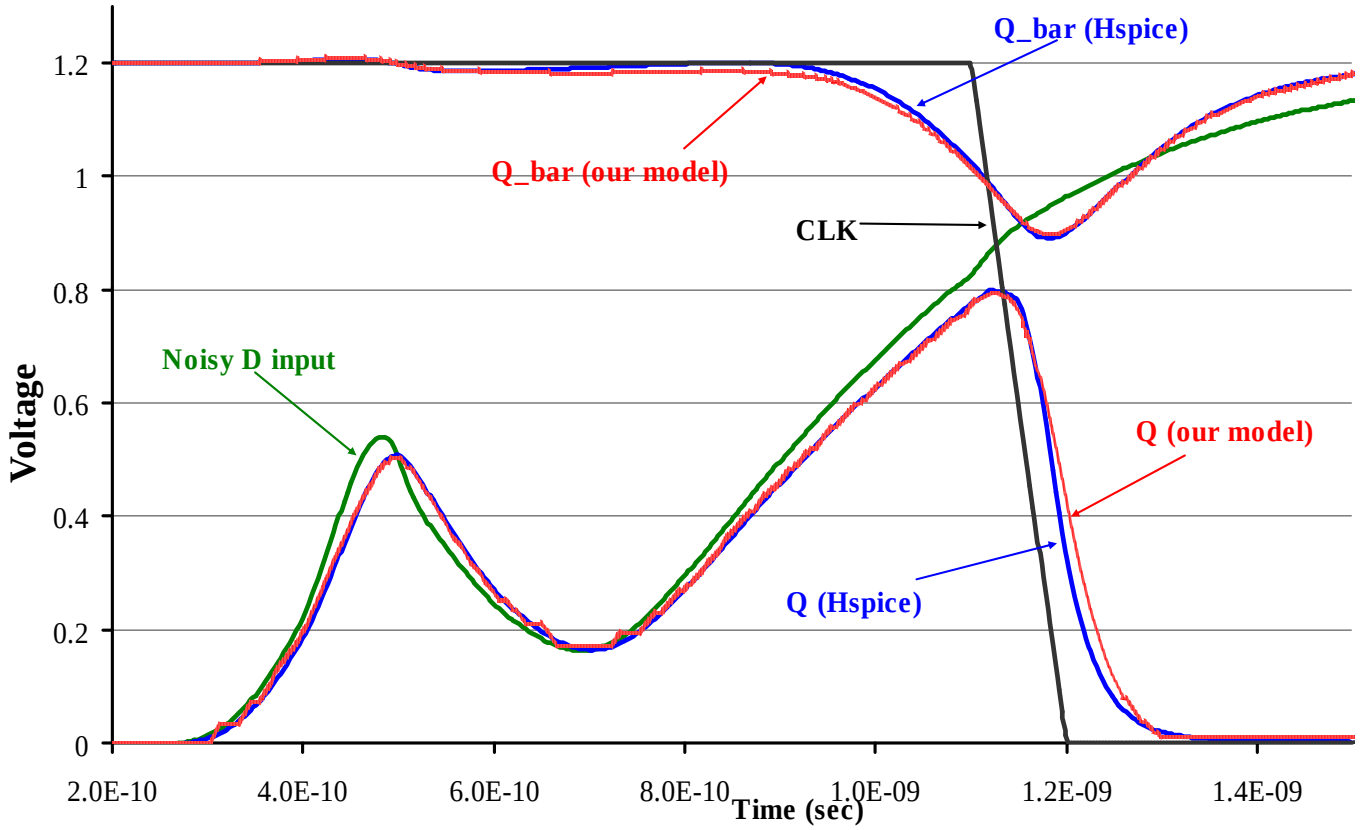
Voltage Calculation



Computing $V_{Q\_bar}(t_{k+1})$:

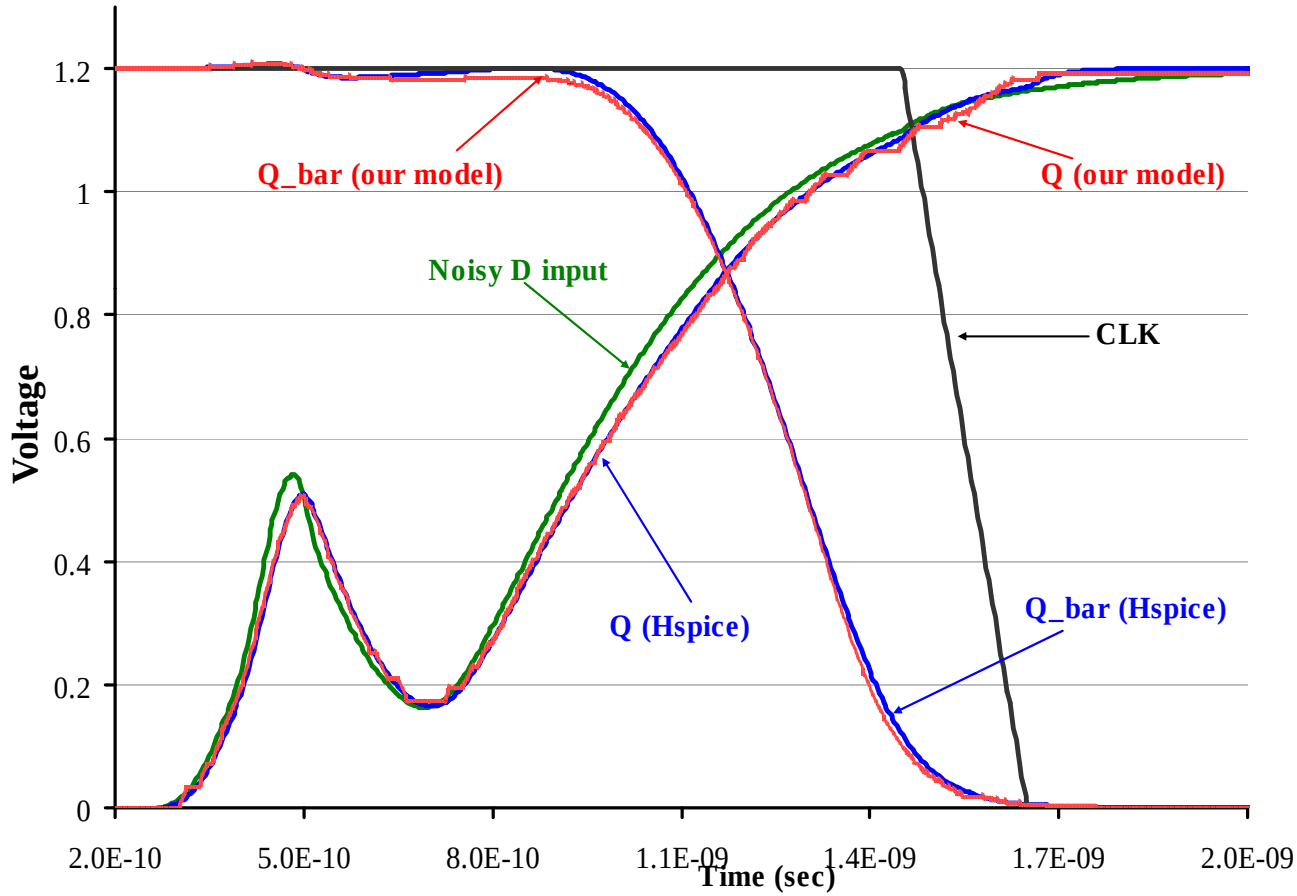
$$V_{Q\_bar}(t_{k+1}) - V_{Q\_bar}(t_k) = \frac{I_{Q\_bar}\left(V_Q(t_{k+1}), V_{Q\_bar}(t_k)\right)\cdot\Delta t + C_M\left(V_Q, V_{Q\_bar}\right)\cdot\left(V_Q(t_{k+1}) - V_{Q\_bar}(t_k)\right)}{C_{Q\_bar}\left(V_Q, V_{Q\_bar}\right) + C_M\left(V_Q, V_{Q\_bar}\right) + C_L}$$

Simulation Results



- (Non-inverting) latch output does not change; noise causes a functional error

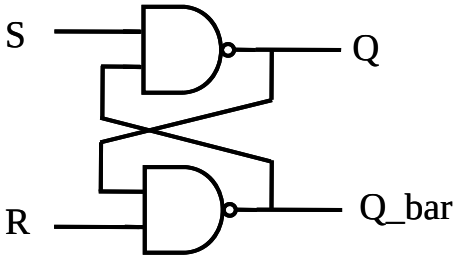
Simulation Results

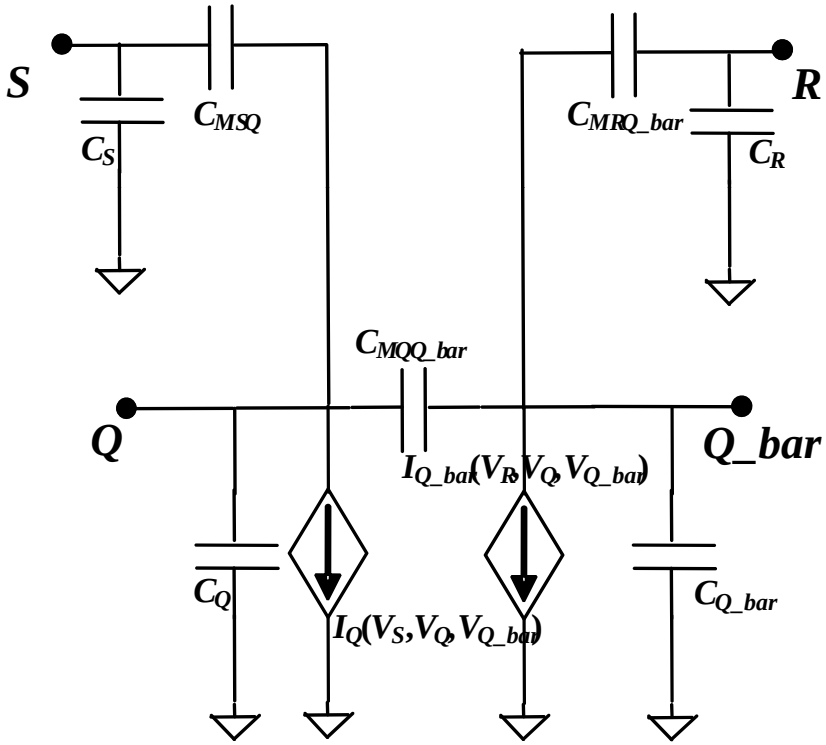


- (Non-inverting) latch output changes as expected; no functional error occurs

SR Latch

- Need to model multiple input switching (MIS)





Simulation Results

- Waveform similarity metric:

$$RMSE = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(V_{SPICE}(t_k) - V_{CSM}(t_k)\right)^2}$$

Library	Cell	Average normalized RMSE		Runtime speedup vs. HSPICE
		Q	Q_bar	
130nm	Latch 1	13.5e-3	11.1e-3	1220
	Latch 2	14.1e-3	12.2e-3	1220
	Latch 3	26.5e-3	23.3e-3	2130
	FF1	6.5e-3	7.3e-3	1110
90nm	Latch 1	12.5e-3	10.1e-3	1230
	Latch 2	14.5e-3	12.8e-3	1330
	Latch 3	27.4e-3	23.6e-3	2160
	FF1	6.9e-3	7.9e-3	1150
65nm	Latch 1	12.9e-3	10.6-3	1290
	Latch 2	14.7e-3	13.3e-3	1290
	Latch 3	27.5e-3	24.5e-3	2170
	FF1	7.6e-3	8.2e-3	1410

Conclusions

- A new current-based cell delay model was developed to accurately capture
  - Various cell parasitic effects
  - Cell nonlinear behavior
- We utilized our CSM-based waveform calculator for the purpose of short circuit current calculation
- CSM for some Sequential cells was introduced
- CSM for multiple input switching considering the stack effect will be developed
- Statistical CSM will be investigated