Analysis of Jitter due to Power-Supply Noise in Phase-Locked Loops

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OUTLINE

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INTRODUCTION

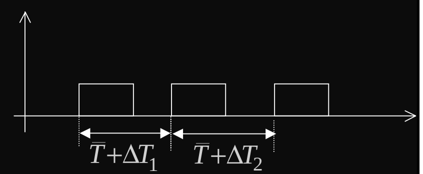
- PLLs are ubiquitous in RF and mixed signal circuits
- The phase-lock concept is fundamental in any situation where some form of feedback is used to synchronize some local periodic event with some observable external event
- Most high-speed microprocessors and memories employ phase locking to suppress timing skews

PLL APPLICATIONS

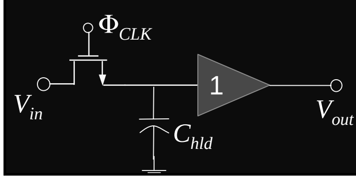
- Clock and data recovery
- Clock generation for microprocessors
- Frequency synthesis
- Demodulation of FM signals
- Coherent demodulation of AM signals
- Local oscillator design for cellular phones, cable modems, and radios

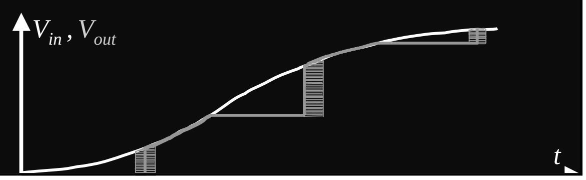
PLL DESIGN SPECIFICATIONS

- Lock range
- Capture range
- Acquisition time
- **Jitter**
  - Cycle-to-cycle jitter:



- The PLL timing jitter can cause serious problems in a system which uses the PLL

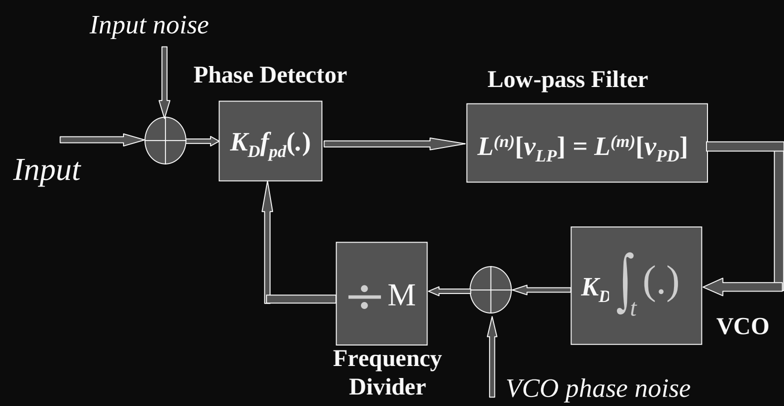




PRIOR WORK

- Oscillator phase noise due to the device noise
  - Using an LTI feedback system approach to analyze the phase noise (*Razavi, JSSC'96*)
  - Using an LTV model and stochastic differential equations to analyze the phase noise (*Hajimiri, JSSC'98*) (*Demir, DAC'98*)
- Oscillator jitter due to power supply noise
  - Using a deterministic frequency modulation model (*Hertzel, CICC'98*)

NOISE SOURCES IN PLL

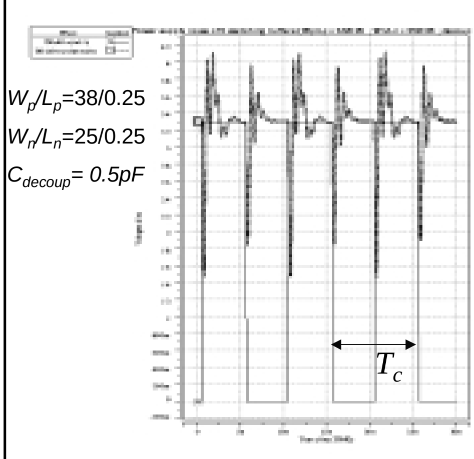


$$L^{(m)} = b_m \frac{d^m}{dt^m} + b_{m-1} \frac{d^{m-1}}{dt^{m-1}} + \cdots + b_0$$

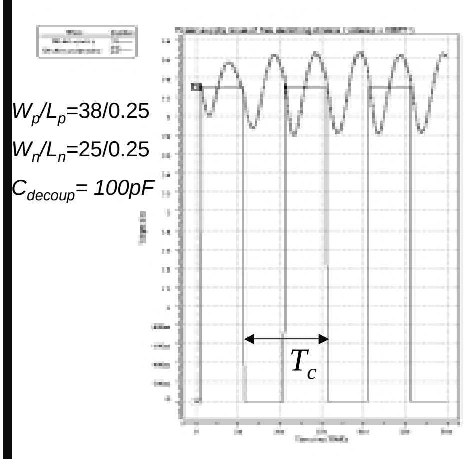
$$L^{(n)} = a_n \frac{d^n}{dt^n} + a_{n-1} \frac{d^{n-1}}{dt^{n-1}} + \cdots + a_0$$

POWER SUPPLY NOISE

Impulsive noise



Sinusoidal noise



MODELING THE SINUSOIDAL NOISE

- When a large decoupling capacitor is present in the circuit, the supply noise is modeled as a sinusoidal waveform with a random maximum amplitude and a uniformly distributed random phase shift in

$[-\pi , \pi]$

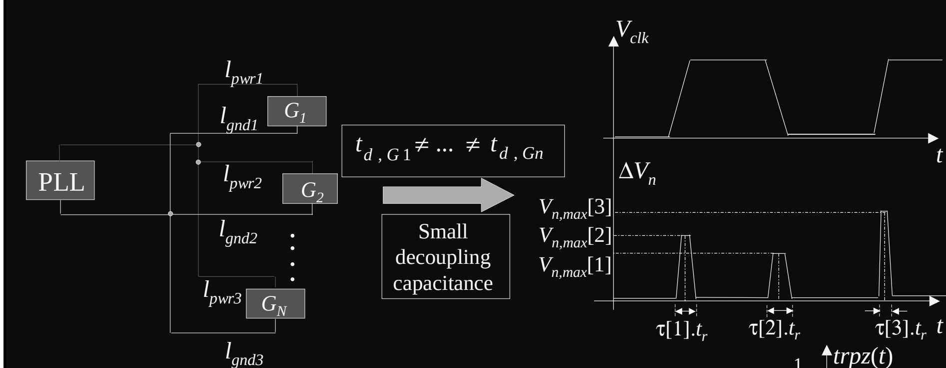
$$V_{n,\max}[k] = V_{n,\max}(kT)$$

$$v_n(t) = V_{n,\max}[k]\sin(\omega_0 t + \theta) \qquad k = 0, 1, 2, \ldots \qquad kT \le t \le (k+1)T$$

- $v_n(t)$ is a wide-sense stationary process, therefore:

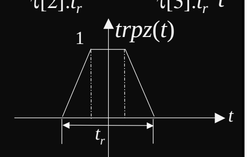
$$\eta_{v_n} = 0 \qquad R_{v_n}(\tau) = \frac{E\{V^2_{n,\max}[k]\}}{t_r}\cos(\omega_0 \tau)$$

MODELING THE IMPULSIVE NOISE



$$v_n(t) = \sum_{k=0}^{\infty} V_{n,\max}[k]\, trpz\left(\frac{t-kT}{\tau[k].t_r}\right)$$

where

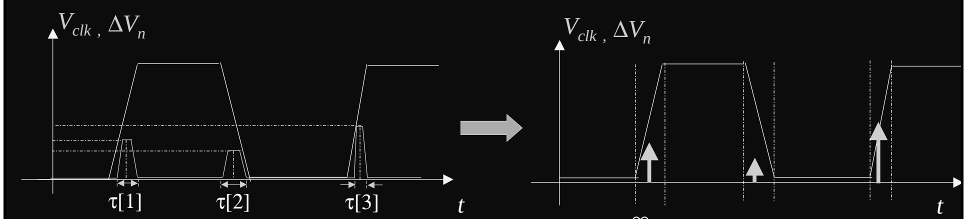


$$kT \le t \le (k+1)T$$

$V_{n,max}[k]$ and $\tau[k]$ are independent stochastic processes.

MODELING THE IMPULSIVE NOISE

- The pulse width of the supply noise is very small compared to the clock period



$$v_n(t) = s(t-\lambda) \qquad \text{where} \quad s(t) = \sum_{k=0}^{\infty} V_{n,\max}[k]\,\delta(t-kT)$$

- When a small decoupling capacitor is present in the circuit, the power supply noise is modeled as an impulse train with a uniformly-distributed random shift in [0 , t_r] and normally distributed random amplitude

MODELING THE IMPULSIVE NOISE

- *s*(*t*) is a wide-sense cyclo-stationary stochastic process

Theorem:

If *s*(*t*) is a cyclo-stationary process and λ is a uniformly distributed random variable in the interval [*0* , t_r] and independent of *s*(*t*), then the process:

$$v_n(t) = s(t - \lambda)$$

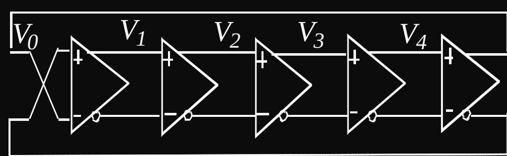
is a stationary process with the following statistics:

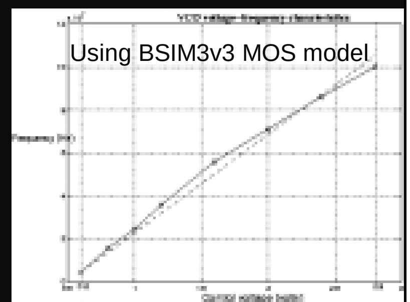
$$\eta_{v_n} = \frac{1}{t_r}\int_0^{t_r} \eta_s(t)\,dt \qquad R_{v_n}(\tau) = \frac{1}{t_r}\int_0^{t_r} R_s(t+\tau,t)\,dt \qquad S_{v_n}(\omega) = \frac{1}{t_r} S_{V_{n,\max}}(e^{j\omega}) \left|X_\delta(\omega)\right|^2$$

$$\eta_{v_n} = E\{V_{n,\max}[k]\} \qquad R_{v_n}(\tau) = \frac{\sigma^2_{Vn,\max}}{t_r}\,\delta(\tau) \qquad S_{v_n}(\omega) = \frac{\sigma^2_{Vn,\max}}{t_r}$$

PHASE NOISE OF THE VCO

- A VCO implemented as a five-stage fully differential ring oscillator exhibits good current-frequency linearity





- The VCO excess frequency is calculated as:

$$\Delta f(t) = \frac{kW\upsilon_{sat}C_{ox}}{2NC_{eq}V_{ref}\left(kW\upsilon_{sat}C_{ox}r_{DS}+1\right)}\cdot v_n(t)$$

PHASE NOISE OF THE VCO

- The autocorrelation of $\Delta f(t)$ is a *linear* function of the autocorrelation of v_n

$$R_{\Delta f}(\tau) = K_{VCO}^2 R_{v_n}(\tau)$$

- The phase noise of the VCO is:

$$S_{\Phi_n}(\omega) = \frac{K_{VCO}^2}{\omega^2} S_{V_n}(\omega) = \begin{cases} \dfrac{K_{VCO}^2}{\omega^2}\cdot\dfrac{\sigma_{V_{n,\max}}^2}{t_r} & \text{Impulsive noise} \\ \dfrac{\pi K_{VCO}^2}{2\omega^2}\cdot\left(\delta(\omega+\omega_n)+\delta(\omega-\omega_n)\right) & \text{Sinusoidal noise} \end{cases}$$

TIMING JITTER OF THE VCO

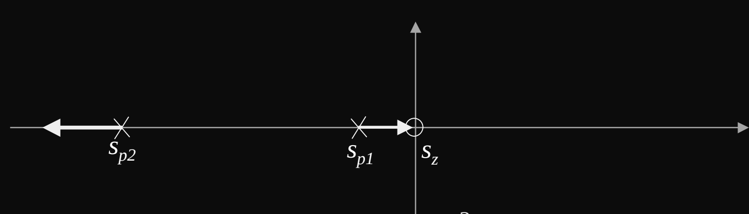
- The timing jitter of the VCO is the standard deviation of the timing uncertainty:

$$\sigma_\tau^2 = \frac{2}{2\pi^2 f_{clock}^2}\left(R_{\Phi_n}(0) - R_{\Phi_n}(\tau)\right) = \begin{cases} \dfrac{K_{VCO}^2}{2\pi^2 f_{clock}^2}\left(\dfrac{\sigma_{V_n,\max}^2 |\tau|}{t_r}\right) & \text{Impulsive noise} \\ \dfrac{K_{VCO}^2}{2\pi^2 f_{clock}^2}\left(1-\cos(\omega_n \tau)\right) & \text{Sinusoidal noise} \end{cases}$$

PLL TIMING JITTER

$$S_{\Phi_0}(\omega) = \left|H_{PLL}(\omega)\right|^2 S_{\Phi_n}(\omega)$$

- Assume that the loop filter is narrowband. Hence the PLL transfer function exhibits a dominant pole



$$S_{\Phi_0}(\omega) = \left|\frac{1/(RK_{PFD})}{1 + (j\omega M)/(RK_{VCO}K_{PFD})}\right|^2 S_{\Phi_n}(\omega)$$

$$s_{p2} = -\frac{RK_{VCO}K_{PFD}}{M}$$

PLL TIMING JITTER (cont'd)

$$jitter_{\Phi_0}(\tau) = \sqrt{\left(\frac{K_{VCO}^2}{2K_{PFD}} \frac{\sigma_{Vn,\max}^2}{sp_2^2 t_r}\right)(1 - \exp(-sp_2|\tau|))}$$

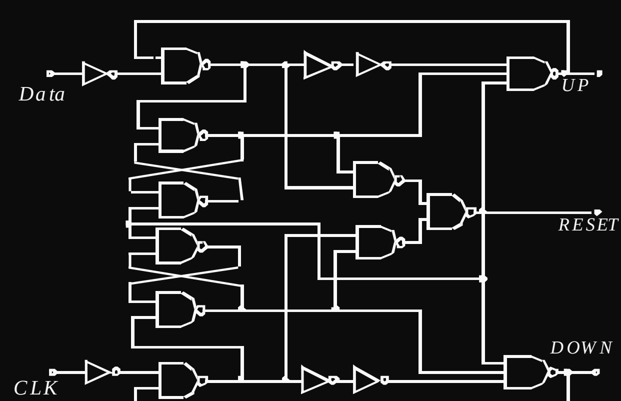
Impulsive noise

$$jitter_{\Phi_0}(\tau) = \sqrt{\left(\frac{K_{VCO}^4}{2\omega_n^2 M^2} \cdot \frac{\sigma_{Vn,\max}^2}{t_r}\right)\left(\frac{1}{\omega_n^2 + sp_2^2}\right)(1 - \cos(\omega_n \tau))}$$

Sinusoidal noise

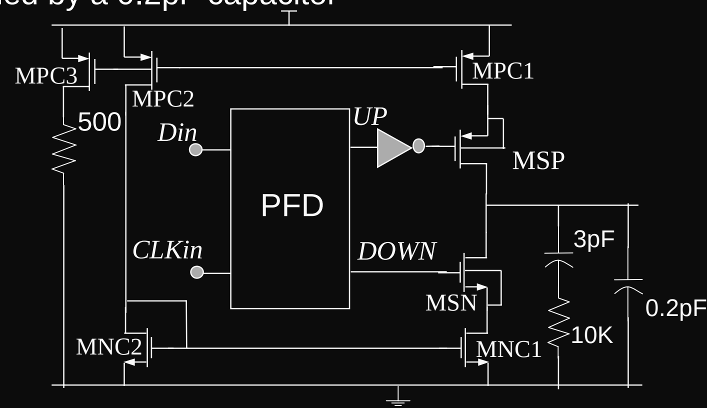
PHASE-FREQUENCY DETECTOR

- Does not suffer from false lock
- The input signal and the VCO output are exactly in phase
- The lock is attained very quickly



CHARGE-PUMP CIRCUIT

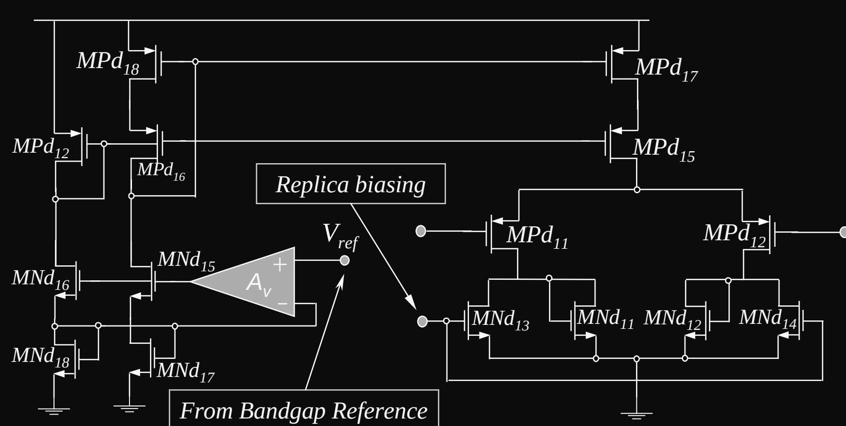
- The zero introduced by the resistor causes a smooth and non-oscillatory transition.
- The glitch produced by the voltage drop across resistor is dampened by a 0.2pF capacitor



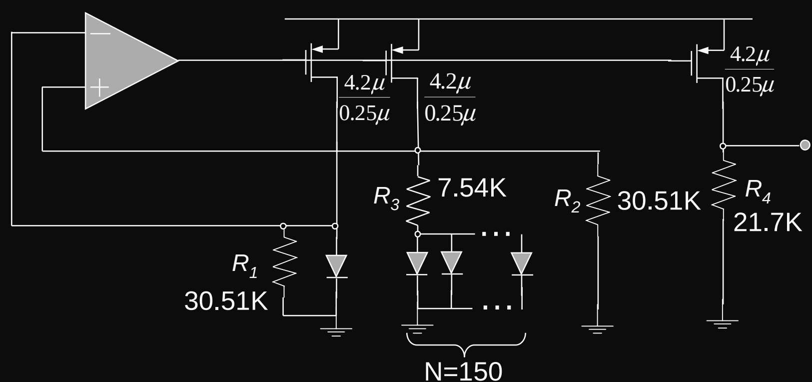
VOLTAGE-CONTROLLED OSCILLATOR

The wide-swing cascode current tail:

1. increases the Power-Supply Rejection Ratio (PSRR)
2. protects the VCO frequency from the supply variations

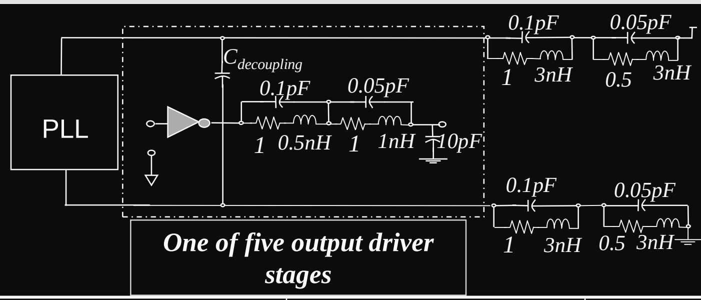


DESIGNOF BANDGAP REFERENCE



- The circuit generates a fixed 0.8V
- It exhibits 0.88% variation in response to a temperature variation of 10-130°C and 0.37% variation in response to a supply variation of 1.8-3.2V

EXPERIMENTAL SETUP



Frequency offset (kHz)	Phase noise [dB/Hz] Analytical	Simulation [dB/Hz]
5.3	-92.2	-93.4
9.1	-96.4	-97.5
15.7	-100.3	-103
32.3	-109.3	-111.2
40	-110	-111.4
64	-112.4	-114.3
80	-115.6	-116.2
100	-119.7	-121.8

CONCLUSION

- A mathematical model for calculating the power supply noise induced timing jitter in PLLs was presented
- The model relies on the stochastic modeling of the power supply noise
- The effect of the power supply noise on the phase noise of the VCO was analyzed and expressed in closed form
- The PLL timing jitter was determined using the phase noise of the VCO
- A PLL was designed and our mathematical model was utilized to predict the timing jitter
- Experimental results show the accuracy of our model