Energy Optimal Sizing of FinFET Standard Cells Operating in Multiple Voltage Regimes Using Adaptive Independent Gate Control

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ABSTRACT
FinFET has been proposed as an alternative for bulk CMOS in the ultra-low power designs due to its more effective channel control, reduced random dopant fluctuation, higher ON/OFF current ratio, lower energy consumption, etc. The characteristics of FinFETs operating in the sub/near-threshold region are very different from those in the strong-inversion region. This paper introduces an analytical transregional FinFET model with high accuracy in both subthrehold and near-threshold regions. The unique feature of independent gate controls for FinFET devices is exploited for achieving a tradeoff between energy consumption and delay, and balancing the rise and fall times of FinFET gates. This paper proposes an effective design framework of FinFET standard cells based on the adaptive independent gate control method such that they can operate properly at all of subthreshold, near-threshold and super-threshold regions. The optimal voltage for independent gate control is derived so as to achieve equal rise and fall times or minimal energy-delay product at any supply voltage level.

Categories and Subject Descriptors
B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

Keywords
FinFET; near-threshold; independent gate control

1. INTRODUCTION
FinFET device, a special quasi-planar double gate (DG) device, has been proposed as an alternative for the bulk CMOS when technology scales beyond 32nm technology [1][2]. In double-gate FinFET circuits, each fin contains two gates, a *front gate* and a *back gate*. The thickness T_{si} of a single fin equals to the silicon channel thickness. The current flows from the source to drain along the wafer plan. In this structure, each fin is essentially the parallel connection of the *front-gate-controlled FET* and the *back-gate-controlled FET*, both with width H equal to the height of each fin. It is proved in [2][3] that FinFET devices can enhance the energy efficiency, ON/OFF current ratio, and soft-error immunity compared with bulk CMOS devices. FinFET devices also show better voltage scalability because of less leakage power consumption [3]. We observe that the minimum energy point (MEP) (~200 mV) of FinFET lies in the subthreshold or near-threshold region, which is typically lower than the bulk CMOS circuits (> 300 mV). Therefore, the FinFET devices outperform bulk CMOS devices in ultra-low power designs by allowing for higher voltage scalability.

One of the unique features for FinFET devices is the independent gate control method, i.e., the front gate and the back gate of a FinFET device can be controlled by different voltages, which enables more power margin and flexible circuit designs [5]. Furthermore, due to the capacitor coupling of the front gate and the back gate, the threshold of the front-gate-controlled FET varies in response to the back-gate biasing, and vice versa. Cakici et al. [4] used independent-gate FinFETs in the pull-down network of an SRAM cell to keep the ~20 pA/um standby power budget. The authors of [5] studied gate sizing and negative biasing on the back gate and showed significant power reduction.

Many burst-mode applications require high performance for brief time periods between extended sections of low performance operation [6]. Digital circuits supporting such burst-mode applications should work on both near-threshold regions and super-threshold regions for brief time periods. The characteristics of FinFETs operating in the sub/near-threshold region are very different from those in the strong-inversion region. In this paper, we target at designing a robust FinFET standard cell library that achieves ***equal rise and fall times*** or ***minimum energy-delay product*** at any supply voltage level, including all of the subthreshold, near-threshold, and super-threshold regions.

First, we notice that the conventional FinFET models are expressed in a piecewise fashion with a breakpoint at or near the threshold voltage V_{th}, separating the super-threshold region where the strong-inversion model is applied [7] and the sub-threshold region where the exponential dependency model is applied. We apply the simple empirical model [8] for the FinFETs operating in both the subthreshold and the near-threshold regimes. This model results in a maximum of 7.76% inaccuracy compared with the HSpice simulation results.

Based on the accurate transregional model, we develop the robust FinFET standard cell library operating at multiple supply voltage levels. We exploit the adaptive independent gate control method, i.e., applying different voltage levels for independent gate control at different supply voltage levels. We start from the FinFET gates designed for equal rise and fall times in the super-threshold region. We define two optimization problems of (i) achieving equal rise and fall times and (ii) minimizing energy-delay product of the FinFET circuit at any supply voltage level. The optimal solution of the first problem achieves the minimum circuit delay, but not necessarily achieves the minimum energy-delay product. In the optimal solution of the second problem, the rise and fall times of the FinFET gates are not necessarily balanced. We derive and find the optimal voltage for independent gate control at any supply voltage level, such that objective (i) or (ii) is achieved. Experimental results using ISCAS benchmarks on 32nm Predictive Technology Model (PTM) for FinFETs [9] show that the proposed design optimization framework achieves up to 64% reduction in energy-delay product.

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2. EXPERIMENTAL RESULTS

We test the proposed optimization framework based on adaptive independent gate control on a set of benchmark circuits, including inverter chains and synthesized ISCAS benchmark circuits. We perform simulations on the 32nm PTM for FinFETs.

Figure 1 illustrates the circuit delay optimization results on a 20-stage inverter chain by adjusting V_{BN} under different V_{DD} levels. One can observe that the independent gate control method achieves more significant reduction in circuit delay when V_{DD} is lower (i.e., in the subthreshold or near-threshold regions.) We observe that the circuit delay can be reduced by up to 48.5% when comparing with the same circuit without independent gate control in the subthrehold or near-threshold regions. This circuit delay reduction is achieved through speeding up the N-type FETs that are relatively weaker in the sub/near-threshold regions.

Figure 2 and Figure 3 illustrate the optimization results on the energy-delay product using adaptive independent gate control (applying different V_{BN} voltage values under different V_{DD} levels), on a 20-stage inverter chain and the ISCAS C432 benchmark, respectively. Table 1 show more results on the reduction of energy-delay product using optimal adaptive independent gate control method. We conclude that (i) the energy-delay product of a circuit can be reduced by up to 64% when comparing with the same circuit without independent gate control; (ii) we achieve more significant reduction in energy-delay product when V_{DD} is lower (i.e., in the subthreshold or near-threshold regions) or when the activity factor α is larger.

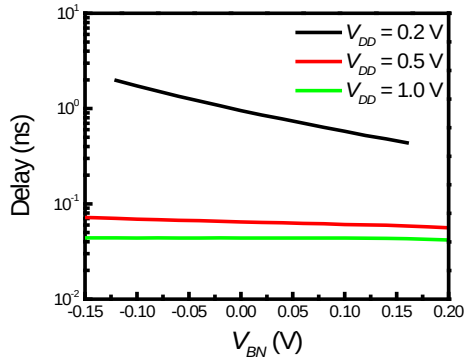

Figure 1. Delay optimization of a 20-stage inverter chain by adjusting V_{BN} under different V_{DD} levels.

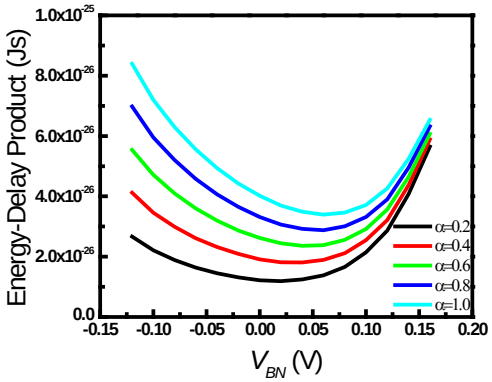

Figure 2. Energy-delay product optimization results on a 20-stage inverter chain by adjusting V_{BN} with different activity factors (V_{DD} = 0.2 V).

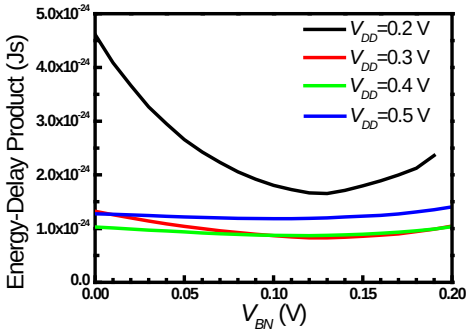

Figure 3. Energy-delay product optimization results of ISCAS85' Benchmark C432 by applying different V_{BN} at different V_{DD} levels.

Table 1. Comparison results on energy-delay product when the adaptive independent gate control method is applied for minimize energy-delay product.

	Baseline (Js)	Optimized (Js)
20-stage inverter chain (V_{DD} = 0.2 V)	4.017×10^{-26}	3.392×10^{-26}
20-stage inverter chain (V_{DD} = 0.3 V)	1.688×10^{-26}	1.518×10^{-26}
C432 (V_{DD} = 0.2 V)	4.615×10^{-24}	1.652×10^{-24}
C432 (V_{DD} = 0.3 V)	1.321×10^{-24}	8.276×10^{-25}
C499 (V_{DD} = 0.12 V)	9.709×10^{-26}	8.660×10^{-26}
C499 (V_{DD} = 0.2 V)	8.124×10^{-27}	7.099×10^{-27}

3. ACKNOWLEDGMENTS

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