Leakage Current Reduction in Sequential Circuits by Modifying the Scan Chains

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4th International Symposium on

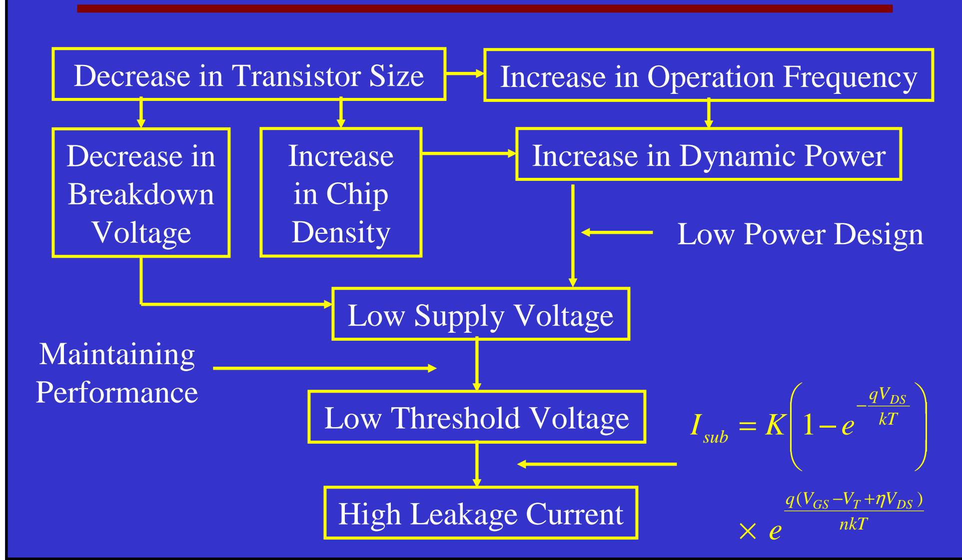
QUALITY ELECTRONIC DESIGN

March 24-26, 2003, San Jose, CA, USA

Outline

- Introduction
- Leakage Reduction Techniques
- Input Vector Control
- Scan Based Testing
- Using the Scan Chain for Leakage Reduction
- Results

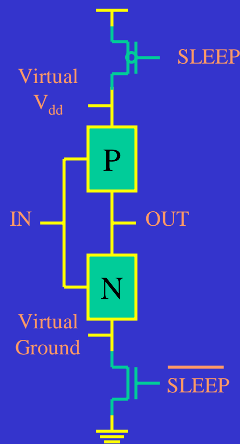
Introduction

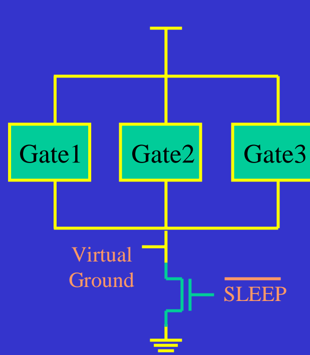


Power Supply Gating

— Low Threshold

— High Threshold





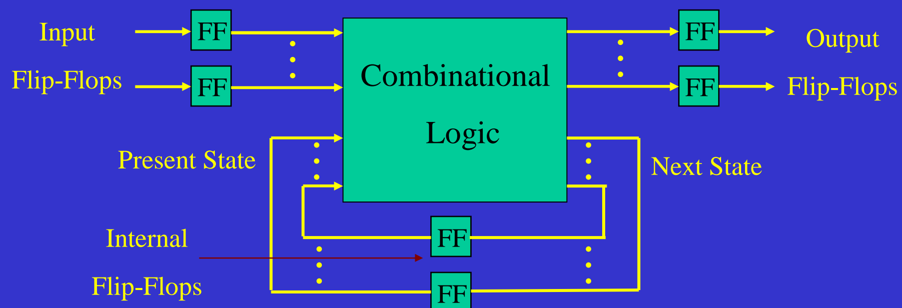
+ Huge reduction in leakage

- Modification in CMOS technology process
- Reduced performance
- Reduced DC noise margin
-Less effective as technology scales down

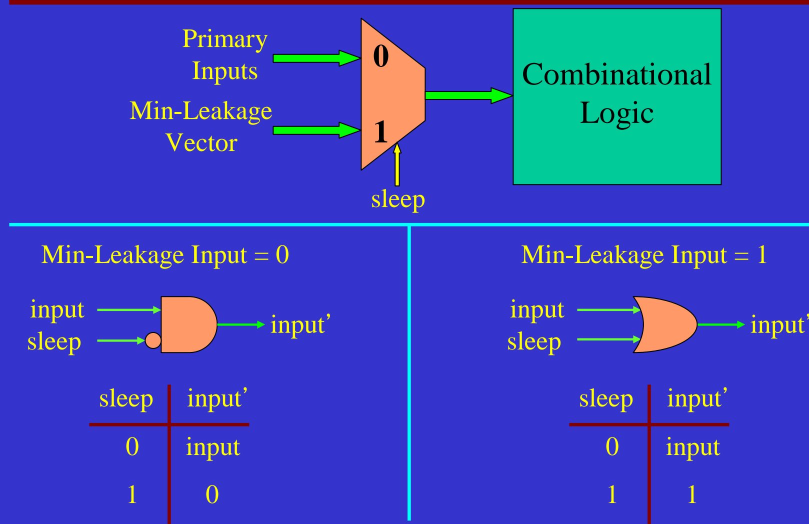
Dual and Variable Threshold Voltages

- Dual Threshold CMOS
  - . High-Threshold devices on non-critical paths
  - . Low-Threshold devices on critical paths
- Variable Threshold CMOS (VTCMOS)
  - . Dynamically change the substrate voltage to control the leakage and speed
  - . Substrate voltage higher than V_{dd} (for P transistors)
  - . Substrate voltage lower than ground (for N transistors)
  - - Requires triple-well technology and additional power supply
  - - Performance penalty (delay of retrieving the substrate voltage)
  - - Less effective with the technology scaling down

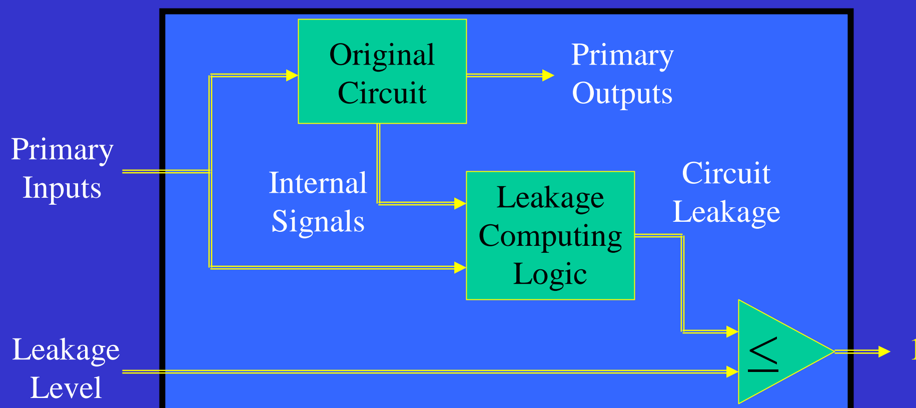
Sequential Circuits



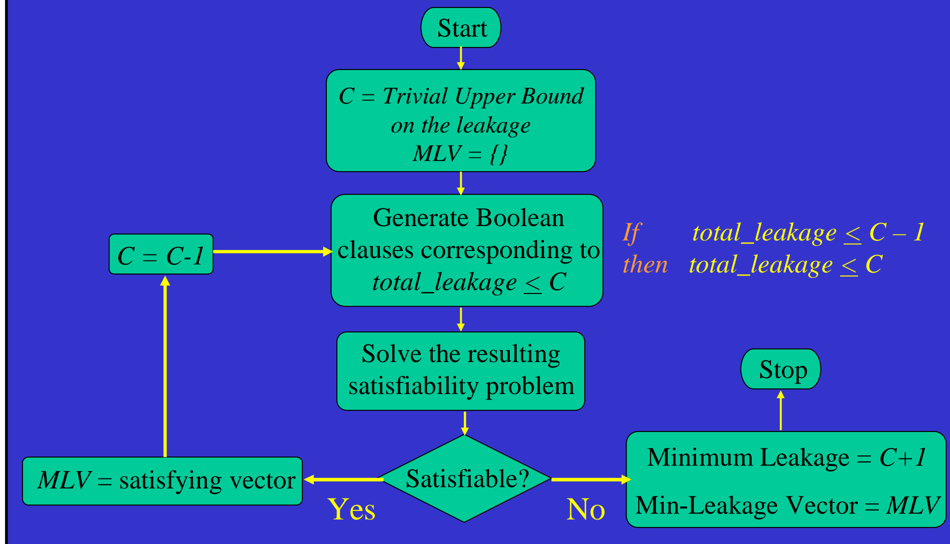
Input Vector Control

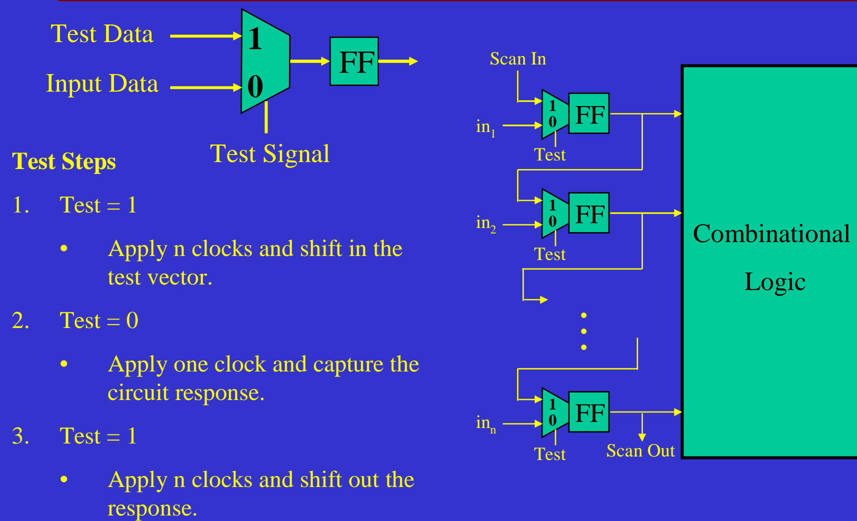


Minimum Leakage Vector Identification

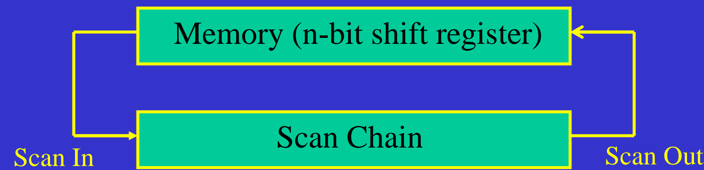


Search for the minimum leakage level for which the above Boolean network is satisfiable.

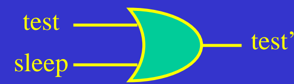

Input Vector Control
Linear Search Algorithm for Minimum Leakage
Start
C = Trivial Upper Bound on the leakage
MLV = {}
Generate Boolean clauses corresponding to total_leakage ≤ C
If total_leakage ≤ C – 1
then total_leakage ≤ C
C = C-1
Solve the resulting satisfiability problem
Stop
Satisfiable?
Yes
No
MLV = satisfying vector
Minimum Leakage = C+1
Min-Leakage Vector = MLV


Scan Based Testing
Test Data
Input Data
1
0
FF
Test Signal
Test Steps
1. Test = 1
• Apply n clocks and shift in the test vector.
2. Test = 0
• Apply one clock and capture the circuit response.
3. Test = 1
• Apply n clocks and shift out the response.
Scan In
in1
in2
inn
Test
FF
Scan Out
Combinational Logic

Using the Scan Chain for Leakage Reduction



Shifting in the *MLV*, from a memory (*n* bit shift register) into the *n* flip-flops via the *ScanIn* pin by setting the circuit into the test mode and applying *n* clocks.

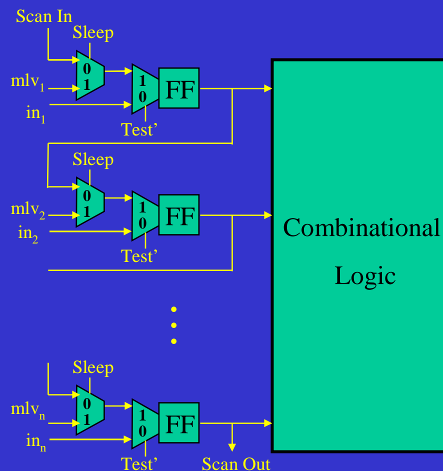


Modifying the Scan Chain

. Sleep mode:
Sleep = 1
Test' = 1
Minimum Leakage Vector is applied to inputs of the combinational logic

. Operational mode:
Sleep = 0
Test' = 0
Inputs directly applied to combinational logic

. Multiplexers are not placed on the critical paths.



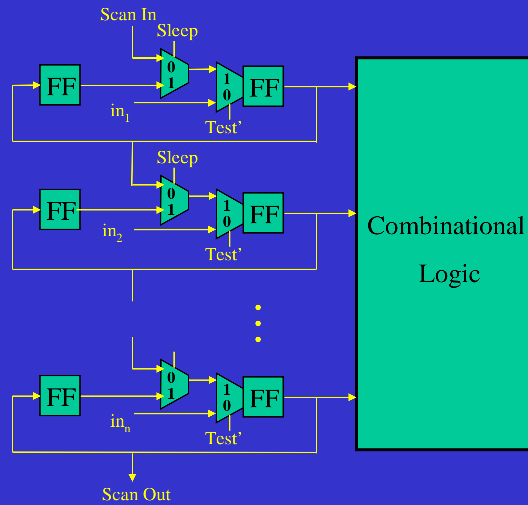
Adding Extra Flip-Flops for State Recovery

Originally MLV is stored in left Flip-Flops.

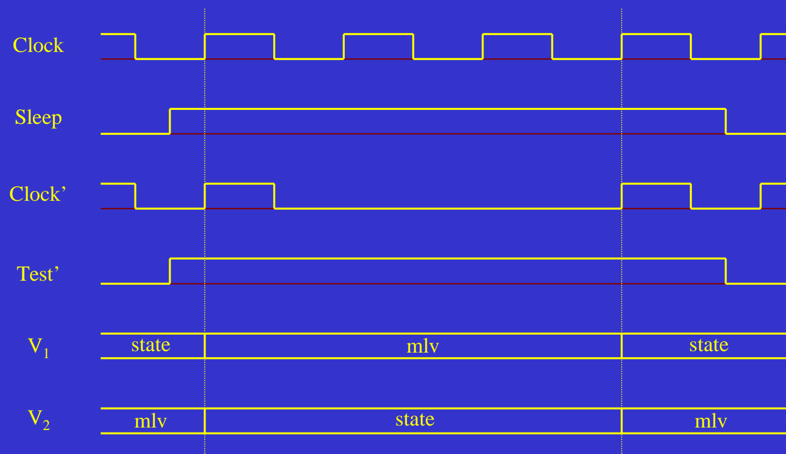
While changing the mode from Sleep to operation and vice versa the content of flip-flops are swapped.

. Sleep mode:
- Sleep = 1
- Test' = 1
- MLV is applied (right FF's)
- State stored in left FF's

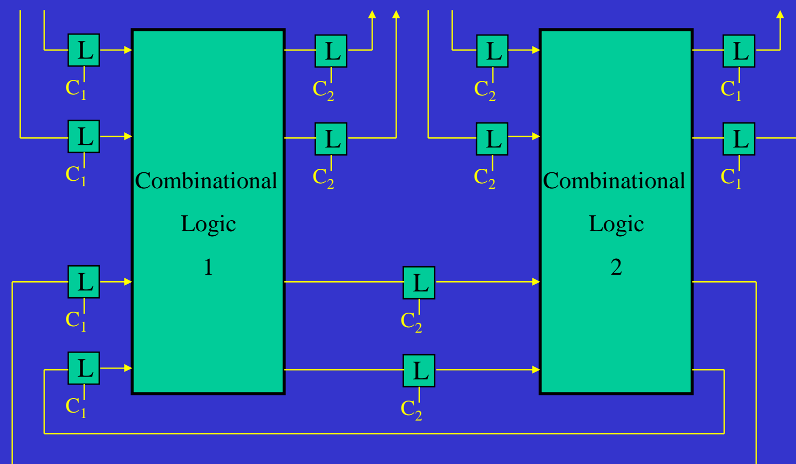
. Operational mode:
- Sleep = 0
- Test' = 0
- Inputs directly applied to combinational logic
- MLV stored in left FF's



Timing Diagram of Control and Clock Signals



Single Latch Sequential Circuit



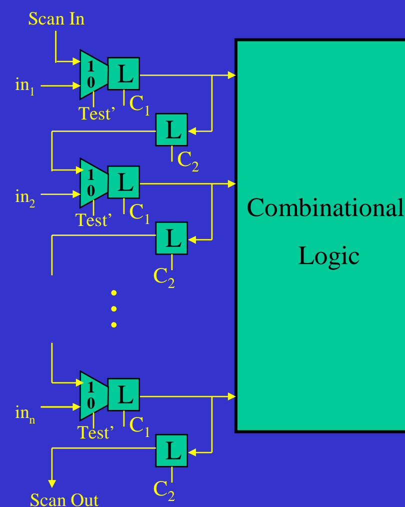
Scan Chain Structure for Single-Latch Sequential Circuits

. Additional multiplexers and latches are added.

. Different phase of clock is used For additional latches.

. In the test mode the original and additional latches make A test chain.

. In the normal mode inputs are directly applied.



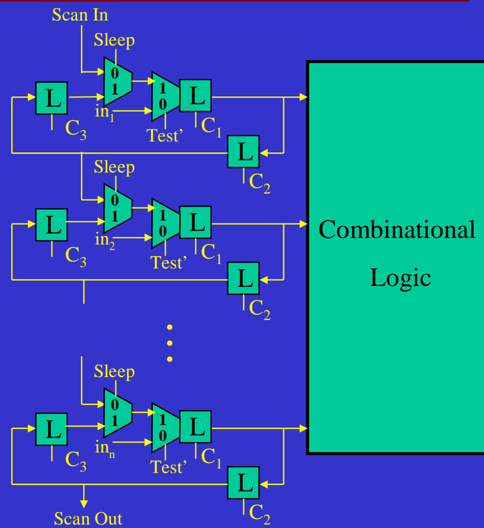
Adding Extra Latches and Multiplexers for State Recovery

. Additional multiplexers and latches are added.

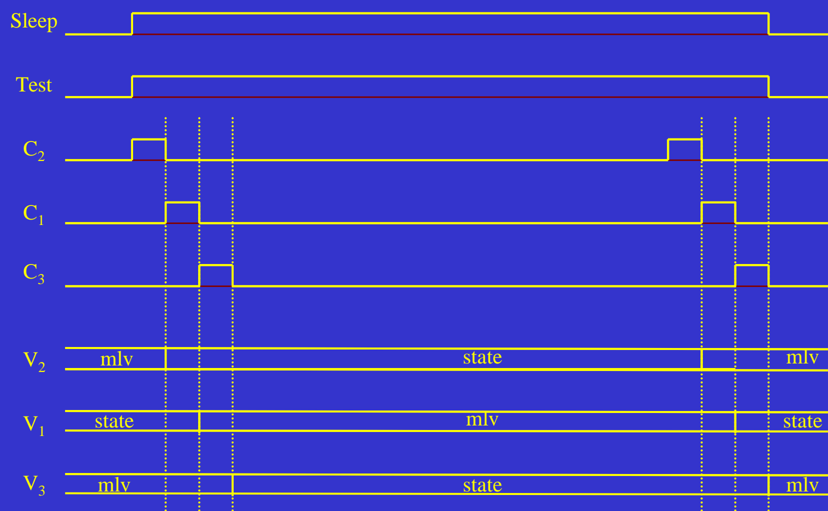
. Originally MLV stored at the latches on the left.

. While changing the mode from Sleep to operation and vice versa the content of flip-flops are swapped

. In the normal mode inputs are directly applied.

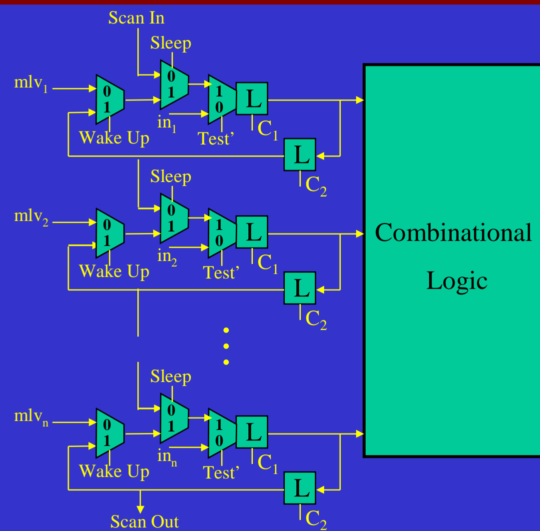


Timing Diagram of Control and Clock Signals



State Recovery without Extra Latches

- Additional multiplexers and no extra latches.
- In the normal mode inputs are directly applied.
- While switching to sleep mode the previous state is stored at extra latches and mlv is applied to the circuit.
- While switching back to the operational mode the previous state is retrieved via the loop



Experimental Results

Circuit	Leakage Reduction	Circuit	Leakage Reduction	Circuit	Leakage Reduction	Circuit	Leakage Reduction
S1196	26%	S35932	16%	S208	36%	S5378	19%
S1238	25%	S382	34%	S27	39%	S641	23%
S1423	19%	S386	27%	S298	35%	S713	31%
S1488	31%	S400	34%	S344	33%	S820	33%
S1494	32%	S510	29%	S349	31%	S838	33%

Minimum: 16%

Maximum: 39%

Average: 29%

Delay Overhead (Proposed versus Standard method)

Circuit	Delay Overhead		Circuit	Delay Overhead	
	Standard	Our		Standard	Our
S1196	10%	1%	S35932	8%	0%
S1238	9%	1%	S382	14%	1.2%
S1423	4%	0%	S386	15%	1.2%
S1488	12%	1%	S400	13%	1.1%
S1494	11%	1%	S510	12%	1%
S208	15%	1.4%	S5378	11%	1%
S27	17%	1.5%	S641	10%	1%
S298	13%	1.2%	S713	9%	1%
S344	12%	1%	S820	12%	1%
S349	13%	1.1%	S838	13%	1.1%

Average Delay for Standard method: 12%

Average Delay for Proposed method: 1%

Conclusion

- Finding the minimum leakage vector
- Modifying the scan chain
- Applying the min-leakage vector to the circuit using the scan chain
  - Flip-Flop circuits
  - Single latch circuits
- Significant leakage saving with negligible performance penalty