Jitter-Induced Power/Ground Noise in CMOS PLLs: A Design Perspective

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Abstract- *CMOS Phase-locked loops (PLL) are ubiquitous in RF and mixed-signal integrated circuits. A general comprehensive stochastic model of the power/ground (P/G) noise in VLSI circuits is presented. This is followed by calculation of the phase noise of the voltage-controlled oscillator (VCO) in terms of the statistical properties of supply noise. Finally the timing jitter of PLL is predicted in response to the VCO phase noise. Next, the design of a low power, 2.5V, 0.25μ CMOS PLL clock generator with a lock range of 100MHz-400MHz is described. Our mathematical mode is utilized to study the jitter-induced power/ground noise. A comparison between the results obtained by our mathematical model and those obtained by HSPICE simulation prove the accuracy of the predicted model.*

1. INTRODUCTION

PLLs are essential wherever a local event needs to be synchronized with a periodic external event. They are utilized as on-chip clock frequency generators to synthesize a low skewed and higher internal frequency clock from an external lower frequency signal. In data communications and disk drive read channels, PLL systems are also used as clock recovery systems. In all of the above applications, the random temporal variation of the phase, or jitter, is a critical performance parameter. In recent years the trend toward increasing clock frequency has made the design of low jitter PLLs even more attractive due to the huge impact of on-chip noise sources (e.g., power/ground noise and substrate noise) on the PLL timing jitter. The increasing demand to integrate all circuit components on the same chip gives rise to some critical noise tolerance requirements for a PLL. The power/ground bounce along with the lower power supply level in the modern VLSI circuits, make the design of low-jitter PLLs a challenging task. Excessively large jitter consumes some of the clock budget and can cause error in the communication links between chips.

The power/ground noise consists of the resistive *IR* drop due to wire resistances and inductive ΔI -noise due to the chip-package wire inductance [1][2][3][4]. In today's deep submicron designs with smaller feature sizes and faster switching speeds, the inductive component of the on-chip interconnect impedance becomes comparable to *R*, and the on-chip power-bus inductance can no longer be ignored. The power supply noise may drive the VCO of the PLL away from its correct frequency, causing the unwanted random uncertainty in frequency, and even making the PLL lose its lock. In the meantime, the supply noise affects the performance of the phase detector and the loop filter. With a careful design of PLL building blocks, the noise contributions of the phase detector, the frequency divider, and the loop filter can be reduced to a tolerable level.

The dominant noise sources are thus the VCO phase noise and the input signal noise. Recently there have been some works on characterizing the phase noise in electrical oscillators [5]. Paper [6] attempts to analyze the timing jitter of oscillators due to the power supply and substrate noise. The oscillator that is subjected to the power/ground noise is considered as a VCO with different control voltages, and therefore the jitter effect is viewed as a frequency-modulated sinusoidal waveform. This paper, however, suffers from one drawback. The VCO system is treated as a deterministic system in the presence of noise. In paper [7] a stochastic model of the power/ground noise for different values of the on-chip decoupling capacitance is proposed. Paper [7], however, does not consider the more general case of having multiple clock frequencies inside the chip.

In this paper we focus on the charge-pump PLL due to its widespread application in today's frequency synthesizers and clock generators for microprocessors. The contributions of the present paper are as follows:

1. Predicting the timing jitter of a PLL in terms of the phase noise of the VCO resulting from the power supply noise. This is accomplished by using a stochastic model for the P/G noise.
2. Designing a low power, 2.5V, 0.25μ CMOS PLL clock generator with a lock range of 100MHz-400MHz and to compare our mathematical model of jitter induced power/ground noise with HSPICE simulation and actual measurement.

Outline of the paper is as follows. In section 2 block diagram of the PLL system in the presence of all relevant noise sources is briefly described. Section 3 gives a statistical modeling of the P/G noise. Section 4 relates the VCO noise to the statistical properties of the P/G noise. Section 5 formulates the effect of the VCO noise source on the output phase of the PLL. Section 6 describes the design of various PLL components. In section 7 the timing jitter and other PLL specifications are measured and presented. Finally, section 8 concludes our paper.

2. SYSTEM MODELING FOR PLL NOISE ANALYSIS

The system block of a PLL along with various random noise sources is shown in Fig. 1. In general all the loop components may contribute to the output noise and accumulated jitter.

The effect of noise on the phase detector performance has been studied in [8]. The phase detectors are not, however, a major source of noise in a PLL [8]. The passive low pass filter introduces thermal and shot noise. The timing jitter due to these device noise sources turns out to be significantly less than that due to substrate and supply noises [7]. As a result, timing jitter is mainly associated with two important noise sources:

- noise at the input,
- phase noise of the VCO.

The loop frequency bandwidth of the system determines which noise source has higher impact on the timing jitter of the output. A narrow loop-bandwidth reduces the impact of the input noise source on the jitter. Previously, more attention has been paid to understanding the effect of the input noise source on the PLL performance. Furthermore, for both clock synthesizers and high performance clock recovery systems, an accurate analysis of the output jitter due to the internal VCO phase noise is important. In this paper, we focus on the VCO phase noise injection into the PLL closed loop system.

3. POWER/GROUND NOISE

Due to the large slew-rates of currents flowing through the pad-pin and pin-package interfaces of the chip packages during the output transitions, the supply and ground lines seen by the on-chip circuitry experience switching noise. Moreover, due to the logic switching of logic circuits inside the chip and abrupt changes in the currents flowing through the supply and the ground wires, the on-chip P/G interconnects experience fluctuations as well. A power supply distribution model must thus include the chip-package-interface power distribution model, the on-chip power bus model, and an equivalent circuit to represent the switching activities in various functional blocks. The fluctuations on the power and rails can have excessively large values when multiple output drivers switch simultaneously.

For convenience, in this paper, we introduce a new terminology for the fluctuations on the P/G lines. The *effective* P/G noise is the algebraic summation of ringings on the power and ground rails. In fact, the effective P/G noise is the main source logic and timing failure in the circuits. To reduce the effective P/G bounce which is a high frequency waveform, the decoupling capacitors have to be placed in close proximity to where the switching is taking place. In practice, designers place the decoupling capacitors at any location that is free after the chip-planning. An on-chip decoupling capacitor can cause the same fluctuations to occur on global power and ground rails. However, it removes high frequency components from the variations and makes the frequency of the oscillations the same as the local clock frequencies. In the time domain, it smooths out the variations on the power and ground wires that would have otherwise been spike-like waveforms. In the frequency domain it shrinks the spectrum of the variations. Paper [9], provides a comprehensive study of the effect of on-chip decoupling capacitors and the mathematical relationship between the peak value of the P/G noise and capacitance value.

Fig. 2. shows the effective P/G noise in the presence of an on-chip decoupling capacitor of 100pF across each output buffer. The device model parameters are taken from the *TSMC 0.25*μ (CM025) single-poly, five-metal CMOS process technology provided by MOSIS which uses the **BSIM3v3** MOS model. Although adding decoupling capacitors largely reduces the spikes on the power and ground rails, it cannot totally eliminate the variations from the rails. Therefore the circuit experiences some degree of bounce effect on the power and ground lines. This bounce influences the VLSI circuit performance, especially in noise sensitive blocks such as on-chip PLL clock generators.

Another problem that needs to be addressed is that different blocks may operate at different frequencies across the chip. The effective P/G noise would thus contain several pseudo-periodic components in different frequencies. This situation is depicted in Fig. 3.

The time-domain waveform for the effective P/G bounce in the presence of decoupling capacitors is an oscillatory waveform. The maximum amplitude of these oscillations is a function of the number of circuits switching simultaneously and the switching activities of the internal circuitry, which itself depends on the nature and statistics of the input signals.

Since the switching blocks are located at different distances from the PLL clock generator, P/G fluctuations due to each switching block will have a different propagation delay to the location of the PLL P/G connections. To account for different propagation delays, we consider the phase shift of the oscillations to be a random process.

As a consequence, the effective P/G noise is modeled as an additive combination of *N* uncorrelated stochastic processes. Each stochastic process represents the effective P/G noise resulting from the switching of circuits within the same block. Each stochastic process contains two independent random variables representing the amplitude and the phase shift of the fluctuation. The random amplitude is modeled as a Gaussian stochastic process [10], whereas the random phase shift is modeled as a uniformly distributed random process. The random amplitude is a discrete-time random process. This is because the circuit switchings occur at different instants of time. Mathematically speaking, the P/G noise can be expressed as follows:

$$v_n(t, k) = \sum^{N} V^{(r)}_{n,max}[k] \sin(\omega^{(r)}_G t + \theta^{(r)}_G) \qquad k \in Z \quad (1)$$

In the above equation, $v_n(t,k)$ is the effective P/G noise which is an oscillatory waveform at intervals of length $T^{(r)}$. $T^{(r)}$ is the local period of each block. $\omega^{(r)}_G$ is the natural frequency of the oscillations. It is determined in terms of the on-chip decoupling capacitance, chip-package interface parasitics, and parasitic components of the on-chip P/G interconnects.

To determine the statistical properties of the effective P/G noise, we first note that $v_n(t)$ is a linear combination of *N* random processes that are mutually uncorrelated:

$$v_n(t, k) = \sum^{N} v^{(r)}_n(t, k)$$

It is easily proved that the statistics of $v_n(t,k)$ are the summation of the statistics of individual processes, $v^{(r)}_n(t, k)$ and that $v_n(t,k)$ is a wide-sense stationary process which has the following first and second-order statistics:

$$\eta_{v_n} = 0 \qquad (2.a)$$

$$R_{v_n}(\tau, 0) = R_{v_n}(\tau) = \sum^{N} \frac{E\left(V^{(r)\,2}_{n,max}[k]\right)}{2} \cos(\omega^{(r)}_G \tau) \qquad (2.b)$$

In the above equation, E(.) represents the expected value of the random process.

4. VCO JITTER ANALYSIS

A VCO that is subjected to the P/G noise generates waveforms with different frequencies. Therefore even in the lock condition, the noisy VCO can generate frequencies that are different from the input signal frequency. From a system perspective, the effective P/G noise is considered as an additive noise source that directly affects the input control voltage. To understand the noise effect of a VCO on the PLL loop operation, consider a four-stage fully-differential ring oscillator-based VCO shown in Fig. 6 [11]. Details of the circuit design of the delay cell are given in section 6.3.

This circuit has a good current-frequency linearity as shown in Fig. 7 [11]. Under these circumstances, the VCO excess frequency is a linear function of the control voltage to the VCO. Using the deep submicron **BSIM3v3** MOS model for the transistors and ignoring the negligible effect of the channel length modulation [12] (shown below):

$$I_D = \begin{cases} kW\upsilon_{sat}C_{ox}(V_{GS} - V_{tn} - V_{DS,sat}) & V_{DS} > V_{DS,sat} \\ kW\upsilon_{sat}C_{ox}\left(\dfrac{1}{1 + \dfrac{V_{DS}}{LE_c}}\right)\left(V_{GS} - V_{tn} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{DS} < V_{DS,sat} \end{cases}$$

the VCO frequency may be expressed in terms of the input control voltage as follows:

$$f(t) = \frac{kW\upsilon_{sat}C_{ox}}{2NC_{eq}V_{ref}(kW\upsilon_{sat}C_{ox}r_{DS} + 1)}(V_{control} - V_{tn} - V_{DS,sat}) \qquad (3)$$

In light of Eq. (3), the autocorrelation of the excess frequency variation is a linear function of the autocorrelation of the effective P/G noise. The inverse Fourier transform of the autocorrelation function of a stochastic process is the power spectrum density of that process. The power spectrum density of the excess phase is referred to as the *phase noise*. Consequently, the phase noise of the VCO is obtained for the P/G noise model:

$$S_{\phi_n}(\omega) = \sum_{r=1}^{N} \frac{\pi K^2_{VCO} E\left(V^{(r)\,2}_{n,max}[k]\right)}{2\omega^2}\left(\delta(\omega + \omega^{(r)}_G) + \delta(\omega - \omega^{(r)}_G)\right) \qquad (4)$$

Taking the inverse Fourier transform gives the autocorrelation as follows:

$$R_{\phi_n}(\tau) = \sum_{r=1}^{N}\left(\frac{K^2_{VCO}}{2\omega^{(r)2}_G} \cdot \frac{E\left(V^{(r)\,2}_{n,max}[k]\right)}{t^{(r)}_r}\right)\cos(\omega^{(r)}_G \tau) \qquad (5)$$

The timing jitter of the VCO is the standard deviation of the timing uncertainty [5], i.e.:

$$\sigma^2_\tau = \frac{2}{(2\pi f_{clock})^2}\left(R_{\phi_n}(0) - R_{\phi_n}(\tau)\right) \qquad (6)$$

Hence the timing jitter for the VCO becomes:

$$\sigma^2_\tau = \sum_{r=1}^{N} \frac{K^2_{VCO}}{2\pi^2 f^{(r)2}_{clock}}\left(1 - \cos(\omega^{(r)}_G \tau)\right) \qquad (7)$$

5. PLL JITTER ANALYSIS

Due to their desirable features (e.g. not exhibiting any false lock, having a fast acquisition-time, and retaining a zero-phase offset in the lock condition), charge-pump PLLs have found widespread use in frequency synthesizer applications where the signal-to-noise ratios are high. The output voltage of the PFD acts like a control voltage for the switched current sources of the charge pump circuit. Finally, the transfer function of the second-order PLL, which uses a simple RC circuit as the lowpass filter, is easily obtained. For the related formulations and derivations see [13]. This familiar formula is presented in Eq. (8) as a reference.

$$H_{PLL}(s) = \frac{\Phi_{out}}{V_N} = \frac{1}{K_{PFD}} \cdot \frac{C_{LP}s}{1 + R_{LP}C_{LP}s + (MC_{LP}s^2)/(K_{VCO}K_{PFD})} \qquad (8)$$

where

$$K_{VCO} = \frac{kW\upsilon_{sat}C_{ox}}{NC_{eq}V_{ref}(kW\upsilon_{sat}C_{ox}r_{DS} + 1)}$$

$$K_{PD} = \left(\frac{I_{CHP}}{2\pi}\right)\left(\frac{1}{\mu_{eff}C_{ox}(W/L)(V_{DD} - V_{th})}\right)$$

Examining the PLL transfer function reveals that the low frequency component of the phase noise of the VCO is attenuated by the closed loop system while the high frequency component of the output follows the variations of the phase noise in the VCO. The system of Fig. 1. is linear and the spectral density of the output due to the VCO phase noise is thus obtained using the transfer function of the system.

$$S_{\phi_o}(\omega) = |H_{PLL}(\omega)|^2 S_{\phi_n}(\omega) \qquad (9)$$

For a second-order PLL the characteristic polynomial is at least a 4th-order polynomial of ω. To simplify the derivations and obtain a closed-form expression, we assume that the loop filter has a narrow bandwidth. Under this assumption, which is valid in most PLL designs, the PLL loop transfer function contains a low-frequency dominant pole. The effect of the dominant pole is approximately canceled out by the zero of the passive LPF in the loop, and hence the PLL loop transfer function is represented by its non-dominant pole. The power spectrum of the output phase is:

$$S_{\phi_o}(\omega) = \left|\frac{1/(RK_{PFD})}{1 + (j\omega M)/(RK_{VCO}K_{PFD})}\right|^2 S_{\phi_n}(\omega) \qquad (10)$$

The autocorrelation function is:

$$R_{\phi_o}(\tau) = \sum_{r=1}^{N}\left(\frac{K^4_{VCO}}{2\omega^{(r)\,2}_G M^2} \cdot E\left(V^{(r)\,2}_{n,max}[k]\right)\right)\left(\frac{1}{\omega^{(r)2}_G + s^2_{p_2}}\right)\cos(\omega_n\tau) \qquad (11)$$

The timing jitter of the PLL is obtained by:

$$j_{\phi_o}(\tau) = \sqrt{\sum_{r=1}^{N}\left(\frac{K_{VCO}^{4}}{2\omega_G^{(r)2}M^2}\,\frac{E\left(V_{n,\,max}^{(r)^2}[k]\right)}{t_r^{(r)}}\right)\left(\frac{1}{\omega_G^{(r)2}+s_{p_2}^{2}}\right)(1-\cos(\omega_G^{(r)}\tau))} \qquad (12)$$

s_{p2} in equations (11) and (12) refers to the non-dominant pole of the PLL which is equal to:

$$s_{p_2} = -\left(\frac{RK_{VCO}K_{PFD}}{M}\right)$$

6. PLL CIRCUIT COMPONENTS

A complete PLL clock generator circuit is designed in 0.25µ CMOS technology. The PLL operates with a lock range from 100MHz up to 400MHz.

6.1. Phase-Frequency Detector

The digital PFD generates a signal that conveys the relative phase and frequency error information. Basically, the PFD is implemented as a finite state machine. Currently, most clock recovery circuits use a phase-frequency detector (PFD). The drawback of some conventional PFDs is a dead-zone in the phase characteristic, which generates phase error in the output signals. To solve this problem, a dynamic CMOS PFD is adopted, as shown in Fig. 4.a, which is similar to the one proposed in [3]. The PFD consists of two half-transparent registers, shown in Fig. 4.b, and a NAND gate. It is triggered by the negative edge of the input signals. The timing diagram of the PFD is shown in Fig. 4.c. Even though the input signals are in-phase, the glitches caused by the reset path always exist. So, extra filters are added in the PFD path to remove the effect of the glitches.

6.2. Charge Pump Circuit

Fig. 2. shows the circuit diagram for the designed charge pump circuit. The charge pump circuit has a differential architecture. A differential charge-pump circuit reduces the ripple on the output control voltage due to the mismatches between magnitudes, durations, or absolute timings of the pairs M1-M2 and M7-M8. To achieve better matching, the critical components were resized, and the layout of the charge pump was designed to be symmetrical. In this circuit schematic the transistor pairs M1-M2 and M7-M8 operate as voltage-controlled switches while the transistor pairs M3-M4 and M5-M6 operate as current sources, which is the opposite form in a conventional charge pump circuit. Thus the well-known problem of charge-injection and clock feedthrough of the output is alleviated. Transistors MN1, MN2, MP1, an MP2 will remove the charges from the nodes pnode1, pnode2, nnode1, nnode2, when UP and DOWN are deactivated, thus causing a large reduction in the static phase offset. Due to the observation in [14], the leakage from nodes pnode1 and pnode2 are larger than those from nodes nnode1 and nnode2. This mismatch in leakage can be compensated by making the gate aspect ratios of MN1 and MN2 1.6-2 times larger than those of MP1 and MP2.

6.3. Voltage Controlled Oscillator

The VCO circuit is very crucial to the total performance of the PLL because the sensitivity of a VCO to coupling noise sources directly contributes to the timing jitter of the PLL. Therefore much attention should be given to design a VCO with a high power-supply rejection ratio (PSRR). A popular way of realizing a digital output VCO is by using ring oscillators.

A four-stage fully-differential VCO is used in the PLL. Fig. 6. shows the circuit structure of the delay stage along with the voltage to current converter. The delay stage consists of six transistors. To have a high differential-gain and guaranteed differential operation, a cross-coupled PMOS pair is used as the active load of the differential delay stage.

Maintaining the 50% duty cycle is important in clock generation applicaion. We adopt the conventional approach in which this goal is achieved by running the VCO at twice the clock frequency and then dividing the VCO output by 2.

7. SIMULATION RESULTS

The experimental setup is shown in Fig. 8. The five inverters are connected to the same voltage and ground lines as the PLL. The drivers switch simultaneously, and the jitter of the PLL due to the P/G is measured. Table 1. shows a comparison of the simulated phase noise levels of the PLL with the measured results. Compared to the measurements, the results are very closed in frequency range where the VCO phase noise is dominant. This shows the validity of our VCO phase noise formulations.

In the next experiment the 2.5V power supply is modulated by a 300mV peak-to-peak, 300MHz band-limited Gaussian noise. The PLL circuit shows a 110ps peak-to-peak jitter.

8. CONCLUSION

This paper presented a mathematical model for calculating the power/ground noise-induced timing jitter in PLLs. The model relies on the stochastic representation of the effective power/ground noise and its effect on the jitter of the VCO and finally the timing jitter of the PLL. Experimental results demonstrate the accuracy of the analytical predictions compared to the measured results. A low-power PLL circuit was designed next. The PLL design favors a 4-stage low-power differential ring oscillator. The peak-to-peak jitter is 110ps under the modulated Gaussian noise with a 300mV peak-to-peak amplitude at 300MHz frequency.

Table 1: Comparison between the simulated and the measured results

Frequency offset (kHz)	Analytical [dB/Hz]	Measured [dB/Hz]
5.3	-68.1	-68.4
9.1	-75.3	-76.5
15.7	-83.8	-84.2
32.3	-88.2	-88.7
40	-93.3	-94.1
64	-98.4	-99.1
80	-101.6	-102.3
100	-111.7	-113.2

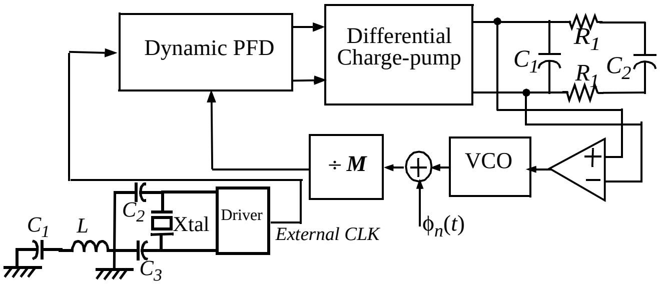


Fig. 1. The functional block diagram of the PLL with the VCO phase-noise source.

Fig. 2. The effective power-supply noise for five identical output drivers switching simultaneously (a 100pF decoupling capacitor is present)

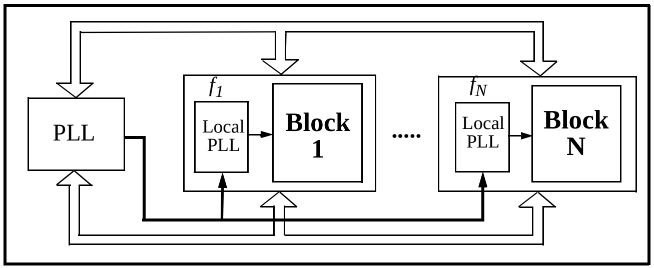
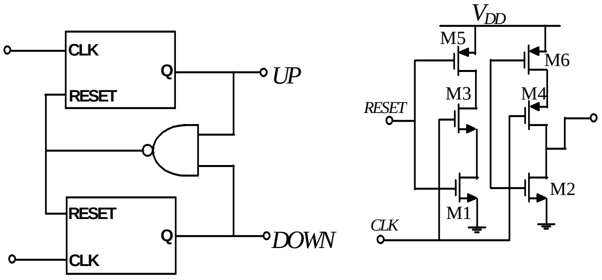


Fig. 3. A simplified schematic of the on-chip global and local clock generators



(a) (b)

Fig. 4. The dynamic phase-frequency detector. (a) The PFD circuit. (b) The circuit realization of the half-transparent register

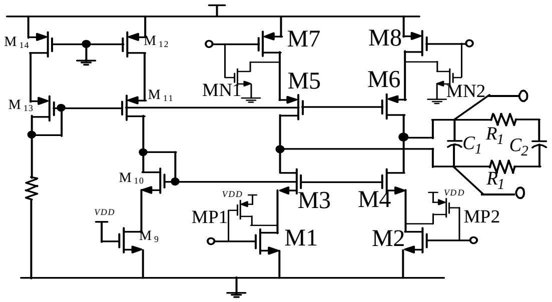


Fig. 5. The charge-pump circuit

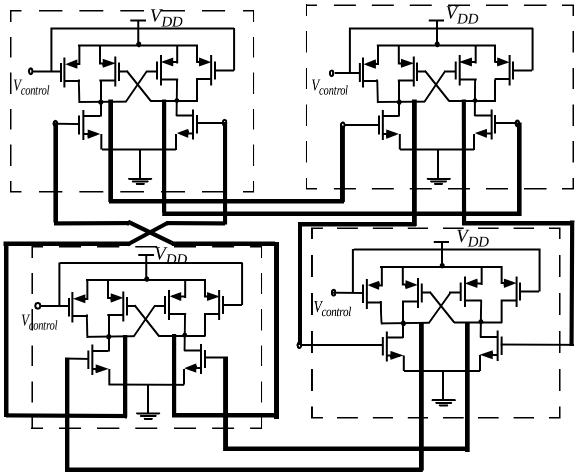


Fig. 6. The VCO based on a four-stage differential ring oscillator.

Bold: Measured
Dotted: Eq. (8)

Fig. 7. The voltage-frequency characteristic of the VCO

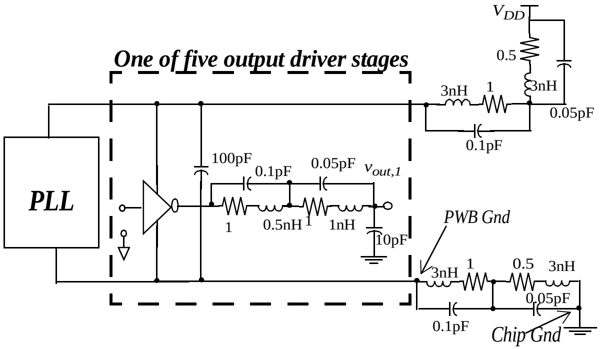


Fig. 8. Experimental setup for measuring the jitter

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