Analysis of Non-Uniform Temperature-Dependent Interconnect Performance in High Performance ICs

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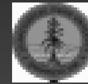

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Presentation Outline

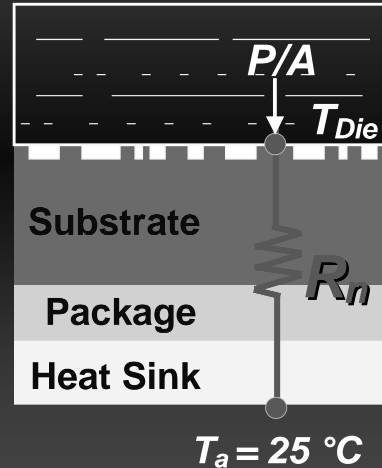
- Introduction
- Analysis of Non-Uniform Chip Temperature
- Temperature-Dependent Interconnect Performance
- Implications for Clock Skew
- Summary

Average Chip Thermal Model

- 1-D heat conduction model

$$T_{Die} = T_a + R_n \left(\frac{P}{A} \right)$$

- Due to excessive Joule heating and the distance from the heat-sink, global interconnect lines are the hottest locations inside the chip

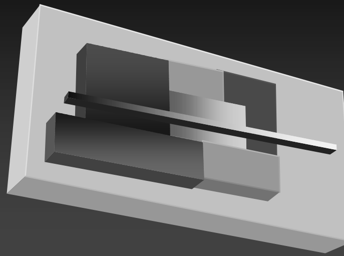


Non-Uniform Substrate Power Map

- Substrate power generation distribution is generally non-uniform
  - Functional block clock gating
  - System-level power management
  - Non-uniform distribution of gate sizing and switching activities in different blocks

Non-Uniform Substrate Temperature

- Substrate thermal profile is non-uniform
  - Thermal time constant is of the order of *ms*
  - Switching activities in the block level are more important
  - Introduces non-uniformity in the global interconnect thermal profile



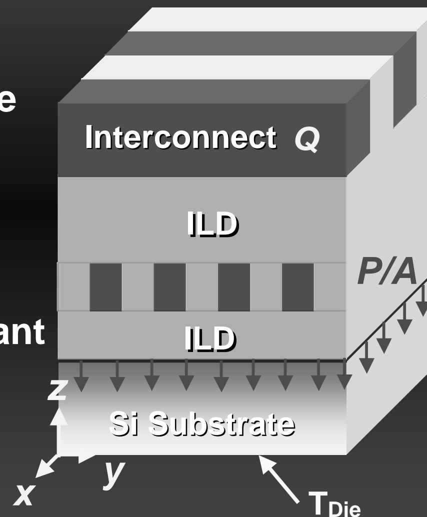
Interconnect Thermal Profile

- Three dimensional heat conduction in steady state

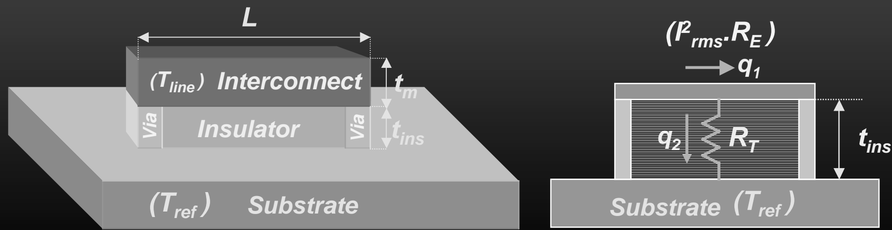
$$\nabla^2 T = 0$$

- With an effective heat generation *Q* in the interconnect and a constant thermal conductivity k_m

$$\nabla^2 T + \frac{Q}{k_m} = 0$$



1-D Heat Equation for Interconnects



$$\frac{d^2T_{line}}{dx^2} = -\frac{Q}{k_m}$$

$Q = q_1 - q_2$

$$\frac{d^2T_{line}(x)}{dx^2} = \lambda^2 T_{line}(x) - \lambda^2 T_{ref}(x) - \theta$$

λ and θ are constants

$f\,(L,\, t_m, k_m, t_{ins}, k_{ins}, I_{rms}, R_E)$

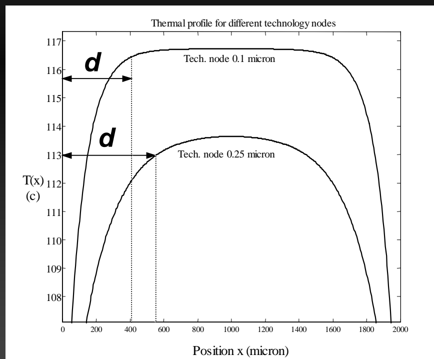
Spatial Temperature Distribution

$L = 2000\ \mu m$

$T(x=0) = 100$ °C

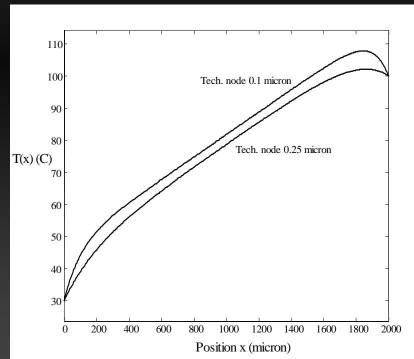
$T(x=2000) = 100$ °C

$T_{ref} = 100$ °C



$T(x=0) = 30$ °C

$T(x=2000) = 100$ °C



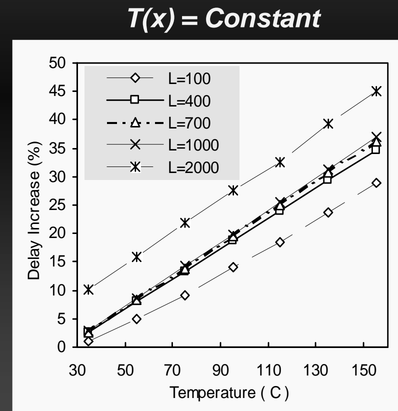
Temperature Dependency of Delay

- Interconnect delay dependent on T due to the T dependence of the resistance

$$r(x) = \rho_0(1 + \beta T(x))$$

- ρ_0 : resistance per unit length at reference temperature
- β : temperature coefficient of resistance (1/°C)

T(x) = Constant



Non-Uniform Temperature-Dependent Delay

- Distributed RC delay model

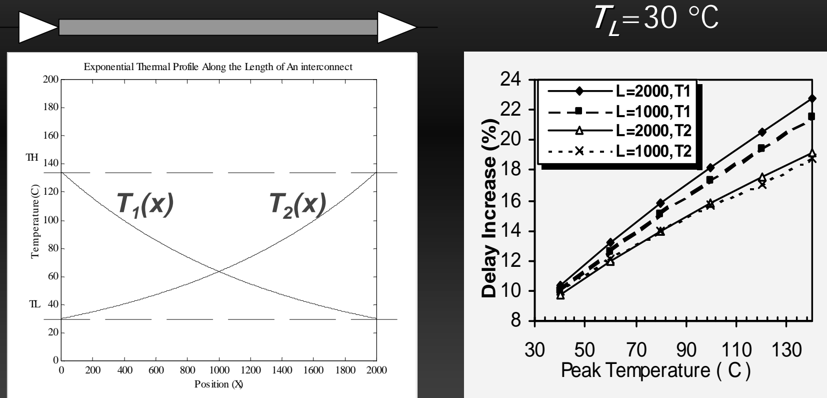
$$D = R_d(C_L + \int_0^L c_0(x)dx) + \int_0^L r_0(x)(\int_x^L c_0(\eta)d\eta + C_L)dx$$

$$D = D_0 + (c_0 L + C_L)\rho_0\beta\int_0^L T(x)dx - c_0\rho_0\beta\int_0^L xT(x)dx$$

D_0 is the Elmore delay model at reference temp.

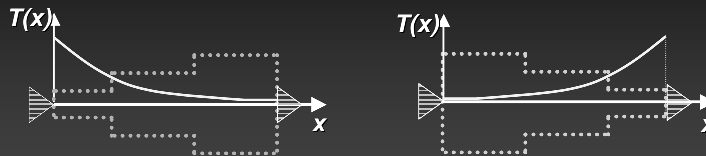
Effects of Non-uniform Thermal Profiles

- Assume two exponential thermal profiles:



Direction of Thermal Profiles

- Decreasing (increasing) thermal profile is equivalent to increasing (decreasing) sizing profile for uniform resistance wire
- Increasing thermal profile has better performance than that of decreasing thermal profile (optimal wire sizing)

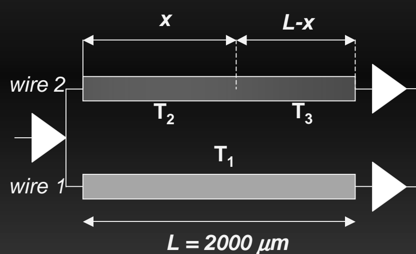


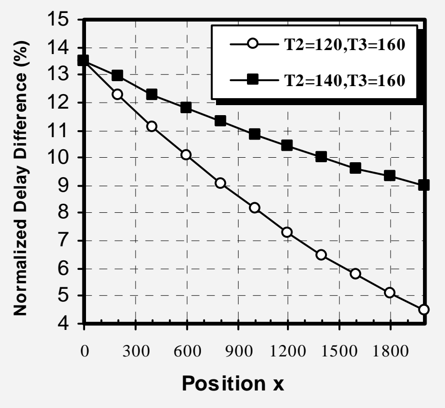
Clock Net Routing

- Clock is the most vulnerable signal to the underlying thermal non-uniformities
  - Usually driven by the highest current
  - Have long global segments in the highest metal layers
- Clock nets must have near-zero skew among their sinks to guarantee correct functionality of the circuits
- Designing with a worst-case uniform-temperature is not sufficient from the clock net point of view

Non-uniform Thermal Effects on the Clock Skew

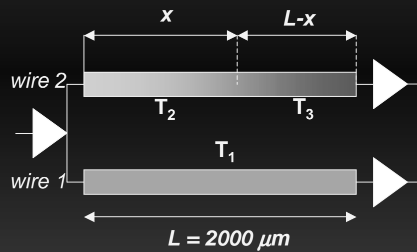
Variable location x, $T_1 = 100$ °C

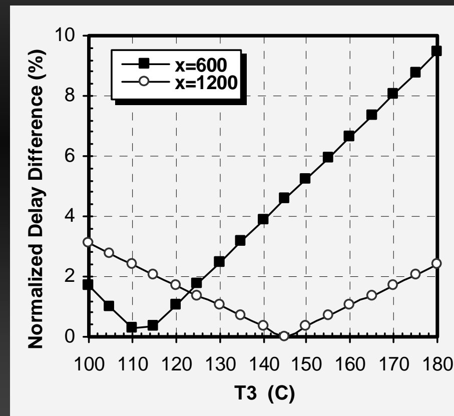




Non-uniform Thermal Effects on the Clock Skew

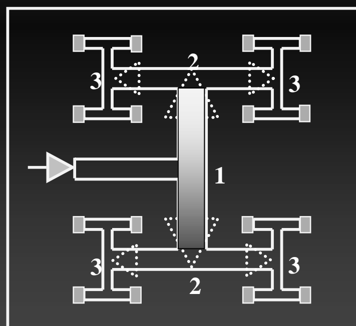
Variable thermal gradient, $T_1 = 100$ °C, $T_2 = 80$ °C





Thermally-Dependent Clock Routing

- Using the proposed delay model, one can modify the bottom-up merging clock routing techniques to achieve near-zero skew (*CICC'01*)



Summary

- Due to different switching activities along with low power design policies, substrate & interconnect thermal maps are non-uniform
- Interconnect thermal non-uniformities:
  - have significant impact on signal performances
  - can introduce significant skew in clock trees
  - may have serious impacts on different EDA flow steps: Buffer-insertion, Buffer-sizing, Gate-sizing, etc.
- Non-uniform interconnect thermal profiles must be considered in the design flow of high-performance VLSI systems