Analysis and Optimization of Power/Ground Bounce in Digital CMOS Circuits

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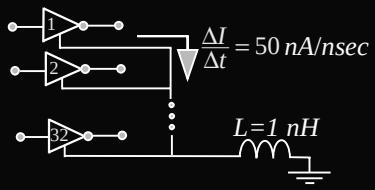
Outline

- Introduction
- Prior Work
- Packaging Technology and Interconnect Levels
- Model of the Chip-package Interface
- Ground Bounce
- Tapered Buffer Design in the Presence of Ground Bounce
- On-chip Decoupling Capacitance
- Skew Control

Introduction

- Signal integrity is a crucial problem in VLSI circuits.
- Package pins, bonding wires, and interconnects cannot be treated as short circuits any more.
- Power/ground bounce limits the performance of high-speed VLSI circuits.
- The noise effects become worse as the clock speed and the number of devices and I/O drivers increase.

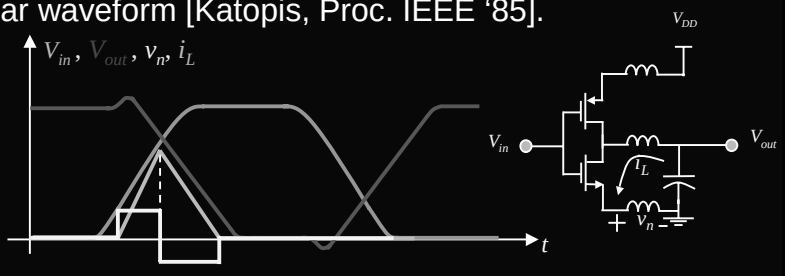


$$NL\ \frac{\Delta I}{\Delta t} = 1.6\ V$$

- Existing models are based on arbitrary assumptions about the form of the current or the ground bounce waveforms.
- Need an accurate and efficient analysis technique for modeling the simultaneous switching noise (*SSN)*.

Prior Work

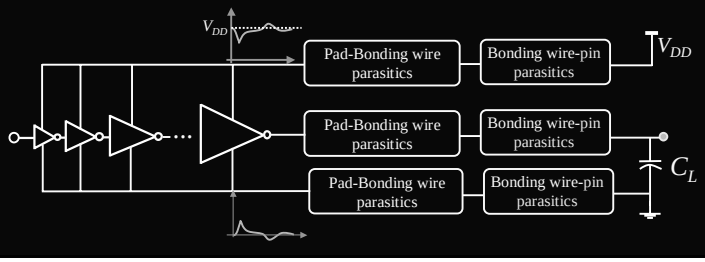
- Current flowing through the output buffers was modeled as a triangular waveform [Katopis, Proc. IEEE '85].



- The square-law current model was used to model the *MOS* transistor and the local negative feedback effect was accounted for [Senthinathan et al., JSSC'91].
- It was assumed that the *SSN* is a linearly increasing function of time [Vaidyanath et al., TCPMT'94].

Prior Work (cntd)

- A methodology was described to analyze the power supply noise [H. H. Chen et al., TCPMT'98]. A power supply distribution model was presented based on:
  - a package level network dominated by inductance,
  - an on-chip power bus network dominated by resistance,
  - an equivalent circuit to represent the switching devices.
  - Triangular or trapezoidal current waveforms for currents.
- The simultaneous switching noise will affect the total delay and transition time of the output buffers [Vemuru, TVLSI'97].



Packaging Technology

- Up to 50% of the delay of a high performance computer is due to packaging delay. This number is expected to rise.
- A good package must comply with a set of requirements:
  1. Electrical requirements
  - Low *R*, *C*, *L* parasitics for pins.

  2. Mechanical and thermal properties
  - High heat-removal rate
  - Good matching between the thermal properties of the die and the chip carrier
  - Strong connection from die to package and from package to board

  3. Cost
  - Cost-performance trade-off
  - Packing density
  - Increasing demand for higher *I/O* count

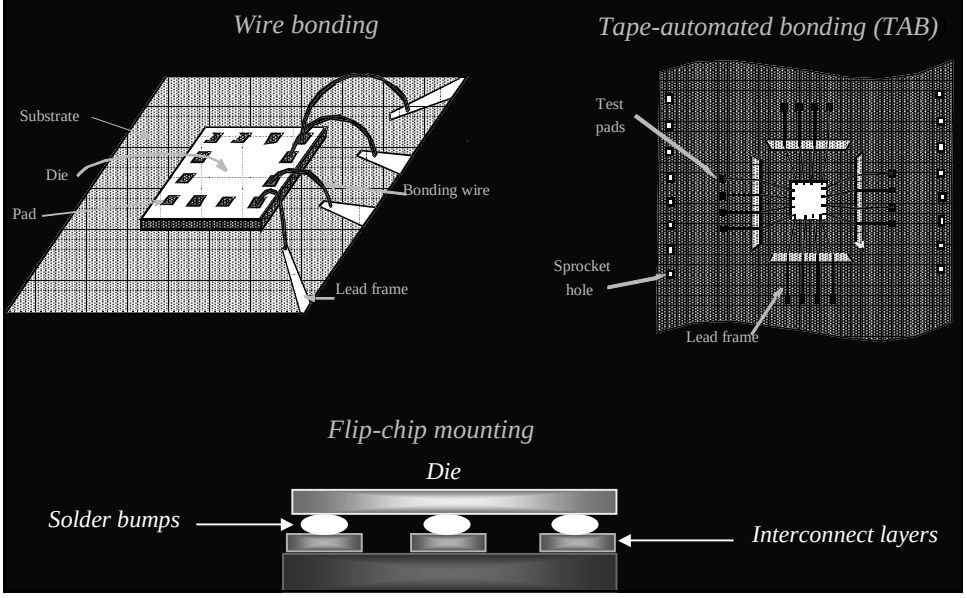
Interconnect Levels

- Conventional packaging approach uses a two level interconnection technology.
- Complex systems may contain even more levels.
- The trend is toward reducing the number of levels

  Solution: Multi-chip modules **(MCM)**

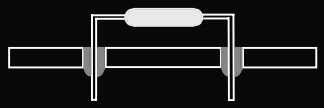
- **Interconnect level 1: Die-to-package-substrate**
  - Wire bonding
  - Tape-automated bonding (*TAB*)
  - Flip-chip

Interconnect Levels

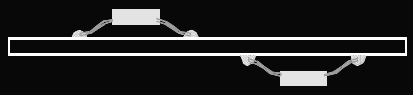


Interconnect Levels (cntd)

- **Interconnect level 2: Package-substrate-to-board**
  - Through-hole mounting
  - Surface-mount



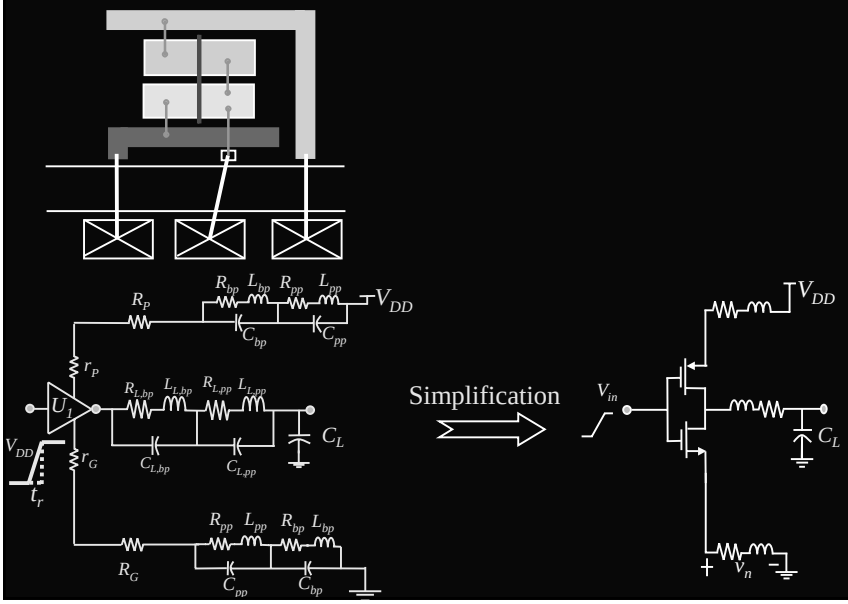
Through-hole mounting



Surface mount

	Wire-bond packaging						TAB packaging			
	40-lead DIP		44-Lead PLCC		132-Lead PQFP		40-lead		132-Lead	
Lead type	Long	Short	Long	Short	Long	Short	Long	Short	Long	Short
Lead length, in	0.99	0.13	0.2	0.15	0.38	0.26	0.12	0.06	0.31	0.23
Resistance, mΩ	125	123	98	98	102	101	3.6	2.2	11	8.2
inductance, nH	22	3.9	4.6	3.3	10	7.2	2.1	0.8	6.7	5.1
Capacitance, pF	0.68	0.12	0.12	0.16	0.21	0.15	0.04	0.02	0.11	0.08

Model of the Chip-Package Interface



Short Channel MOS Device

- With rapid decrease of the feature sizes of the MOS devices, the short channel effects must be accounted for.

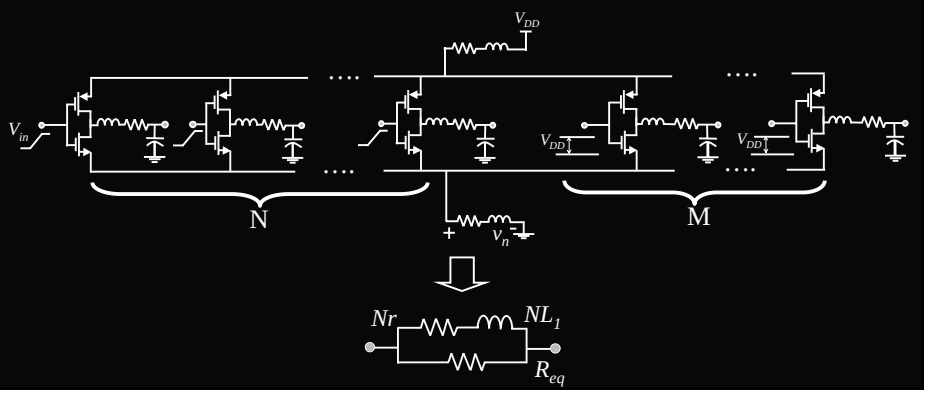
Observations:

- Ignore the effect of channel-length modulation
- L_{eff} is 0.13μ-0.25μ in current technologies. The i_d-v_{ds} equation in the saturation region based on empirical results.
- To come up with a closed form delay expression, the lateral electric field in short-channel transistors is assumed to be a constant in terms of drain-source voltage.

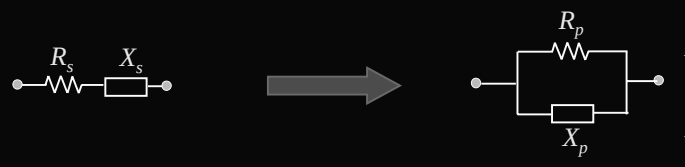
$$i_d = \begin{cases} \beta_n (v_{gs} - V_{tn}) & v_{ds} \geq V_{ds,\,sat} \\ 2\beta_n [(v_{gs} - V_{tn}) - \frac{v_{ds}}{2}] & v_{ds} \leq V_{ds,\,sat} \end{cases} \quad ; \quad \beta_n = \frac{0.5 K_n (W/L)}{1/(V_{DD} - V_{tn}) + 1/LE_c}$$

Ground Bounce

- Assume that *N* output drivers switch simultaneously while the remaining *M* drivers are quiet.
- The quiet drivers are in the linear region.

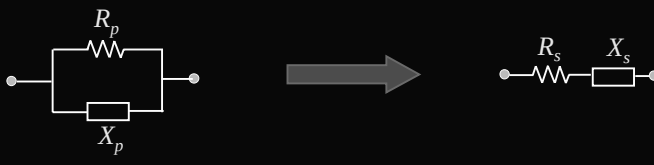


Circuit Transformations



$$R_p = \frac{R_s^2 + X_s^2}{R_s}$$

$$X_p = -\frac{R_s^2 + X_s^2}{X_s}$$



$$R_s = R_p \cdot \frac{X_p^2}{R_p^2 + X_p^2}$$

$$X_s = -X_p \cdot \frac{R_p^2}{R_p^2 + X_p^2}$$

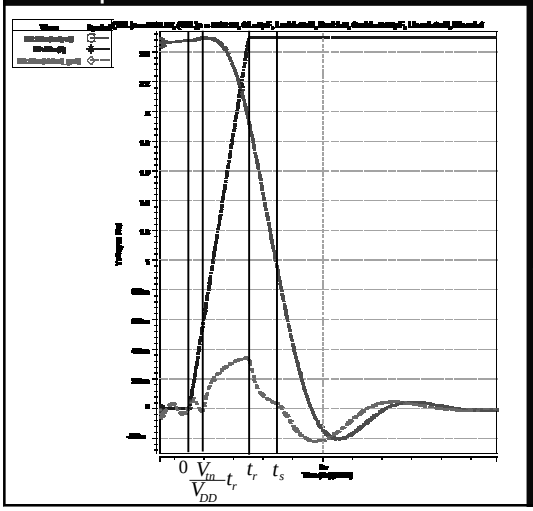
If $R_{eq} >> |N\omega L_1|, Nr_1$, then:

$$L = NL_1\left(\frac{R_{eq}}{Nr+R_{eq}}\right)^2$$

$$R = \left(\frac{Nr\,R_{eq}}{Nr+R_{eq}}\right)$$

Ground Bounce

- The input to the drivers is modeled as a flattened ramp input.



Region $0 \le t \le \frac{V_m}{V_{DD}}t_r$:

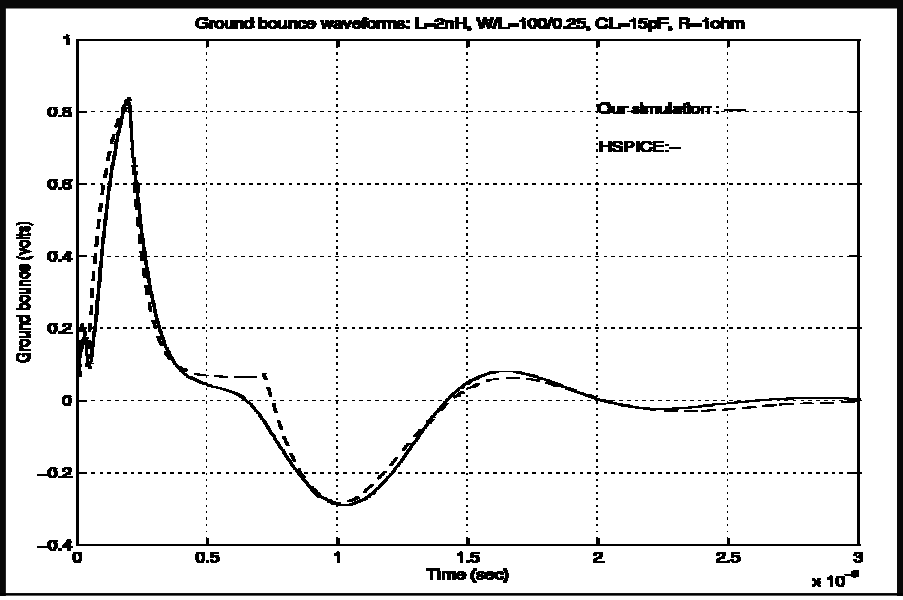
Differential equation:

$$\frac{d^2 v_n}{dt^2} + \left(\frac{R}{L}\right)\frac{dv_n}{dt} + \frac{v_n}{LC_{gs}} = \frac{R}{L}\cdot\frac{V_{DD}}{t_r}$$

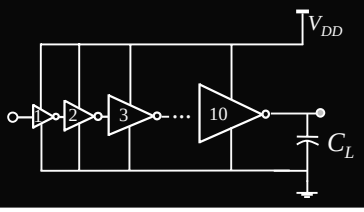
Solution:

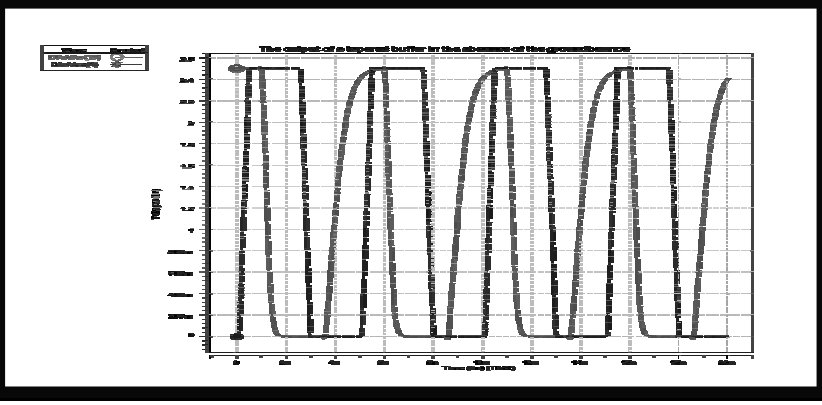
$$v_n(t) = \frac{V_{DD}}{t_r\omega_d}e^{-\alpha t}\sin(\omega_d t) + \left(2\alpha\frac{V_{DD}}{t_r\omega_n^2}\right)\left[1 - \frac{\omega_n}{\omega_d}e^{-\alpha t}\sin(\omega_d t + \theta)\right]$$

Simulation Results

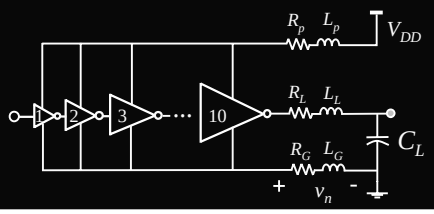


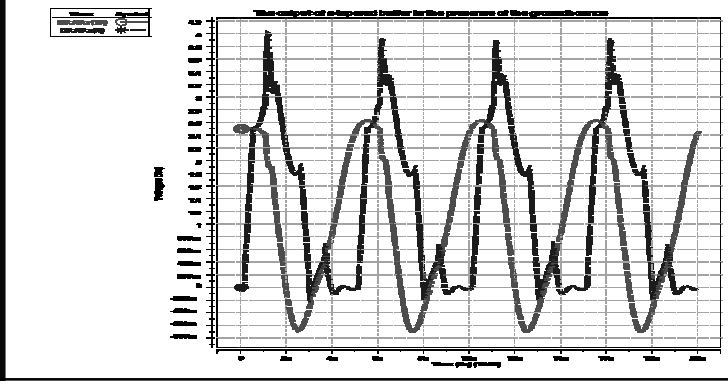
Tapered Buffer Design



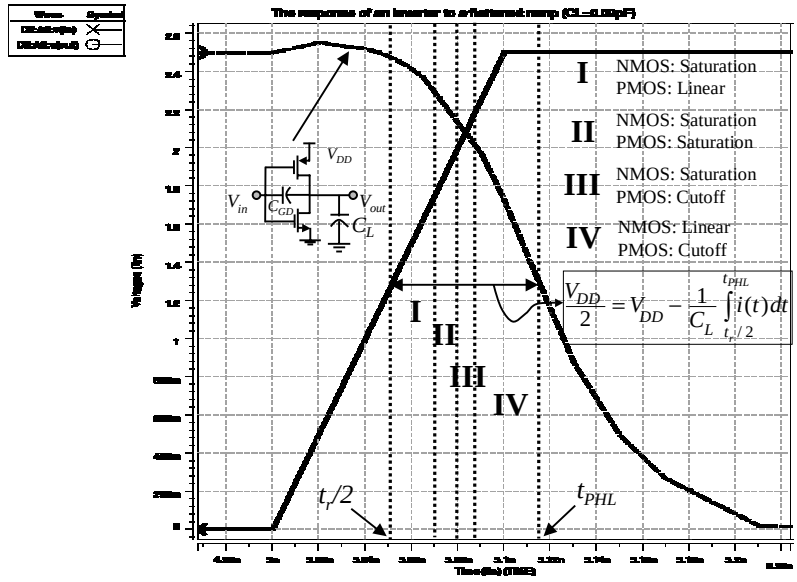


Tapered Buffer Design (cntd)





Regions of Operation



Propagation Delay

$$t_{PHL} = t_{PHL,0} + t_{r0}\left[\frac{1}{4}\left(\frac{1}{2} - \frac{\beta_p}{\beta_n}\right)\left(1 - \frac{2V_T}{V_{DD}}\right) + \varepsilon\right]$$

$$\varepsilon = \frac{1}{2}\left[1 + \frac{1 - V_T/V_{DD}}{1 - 2V_T/V_{DD}}\right]$$

$$t_{PHL,0} = \frac{C_L}{2\beta_n(1 - 2V_T/V_{DD})} - \left[\frac{V_T/V_{DD}}{1 - 2V_T/V_{DD}}\tau \ln\left(\frac{1}{1 - V_T/V_{DD}}\right)\right]$$

$$\tau = r_{DS}(C_L + C_{db,n})$$

- t_{r0} is the input rise-time of the single driver.
- $t_{PHL,0}$ is the 50% propagation delay in the ideal case of having an ideal step input.
- The total propagation delay is: $t_d = \frac{t_{PLH} + t_{PHL}}{2}$

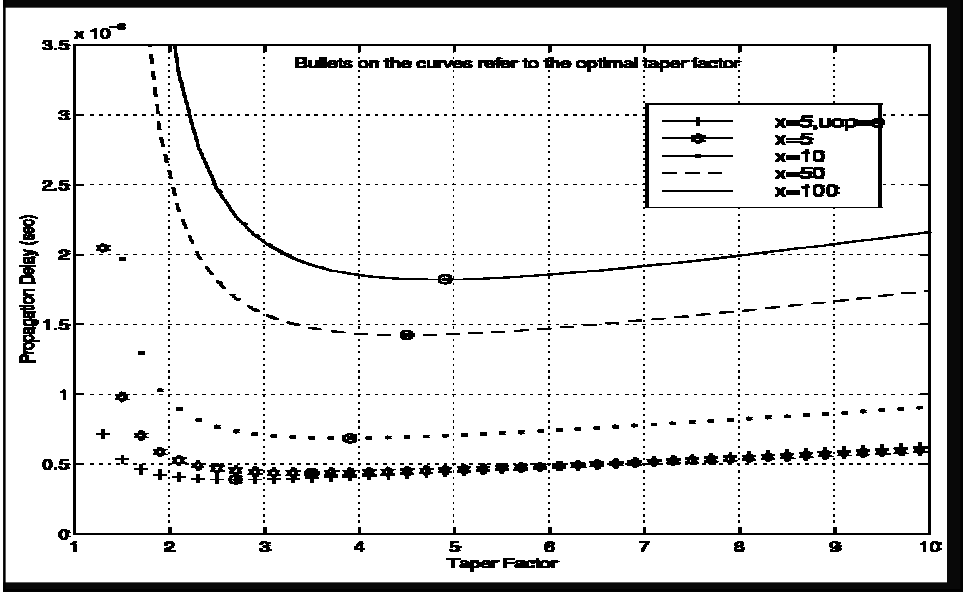
Propagation Delay

- **Lemma 1.**
  1. Suppose that there is a chain of *P* inverters, each consisting of short channel devices.
  2. Assume that the gate aspect-ratio of each stage is *u* times larger than that of the previous stage.
  3. Assume that for $t_{r,i} = \eta t_{d,i} + t_{r,i-1}$ for $2 \le i \le P$ then the total propagation delay is given by:
  4. $$t_p = u\left[\frac{(\eta A + 1)^P - 1}{\eta A}\right]t_{p0} + \left[\frac{(\eta A + 1)^P - 1}{\eta}\right]t_{r0}$$

     where $A = \frac{1}{8} - \frac{1}{8}\left(\frac{\beta_n}{\beta_p} + \frac{\beta_p}{\beta_n}\right)$ and $\le \eta \le 2$

  t_{p0} is the propagation delay of a minimum size inverter when the input rise-time is zero.

Simulation Results



Tapered Buffer Design with Ground Bounce

- First the impact of the ground bounce on the delay of the single buffer is studied.
- To simplify the formulations the pin-package-interface parasitic is modeled by a pure inductor.
- The pure inductive model yields sufficiently accurate result for the optimization problems.
- The propagation delay increases further due to the presence of the ground bounce:

$$t_{p0,\,SSN} = t_{p0} + \frac{\delta}{t_{r0}} \qquad \text{where} \qquad \delta = L^2\left(\frac{\beta_n^2+\beta_p^2}{2}\right)\left(\frac{V_{DD}}{V_{DD}-V_T}\right)$$

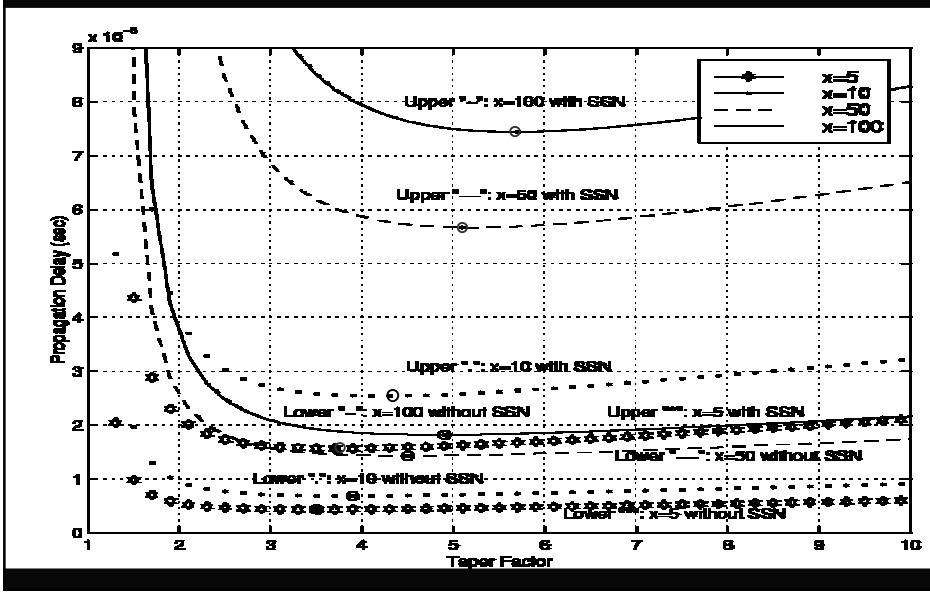
Tapered Buffer Design (cntd)

- **Lemma 2.**
  - For a multistage tapered buffer with the same specification given in lemma 1 and in the presence of the ground bounce, the total propagation delay is obtained by the following equation:

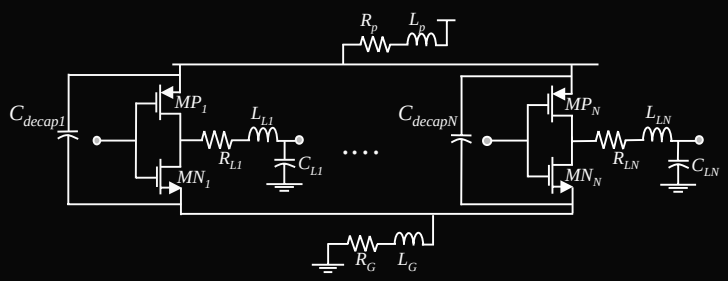
$$t_{p,SSN} = t_{p,initial} + \frac{\delta . A}{(\eta A+1)^{P}\,(ut_{p0,SSN} + t_{r0}) - ut_{p0,SSN}}$$

where $t_{p,initial}$ has the same form as t_p given in previous equation except that t_{po} is replaced with $t_{p0,SSN}$.

Simulation Results

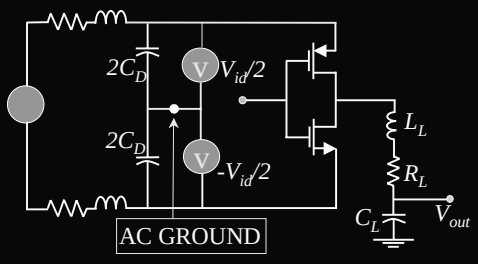


On-chip Decoupling Capacitor

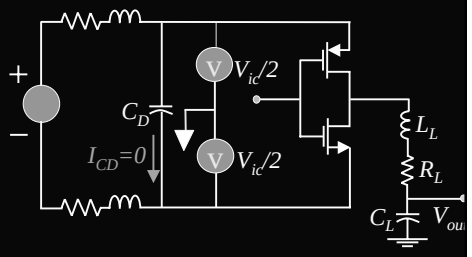


- Need to properly estimate the required amount of the on-chip decoupling capacitors.
- Overestimation is costly from the area point of view.
- Underestimation may lead to noise margin problems.
- The on-chip decoupling capacitor forces the same fluctuations to appear on the on-chip power and ground wires.

Calculation of the Decoupling Capacitance



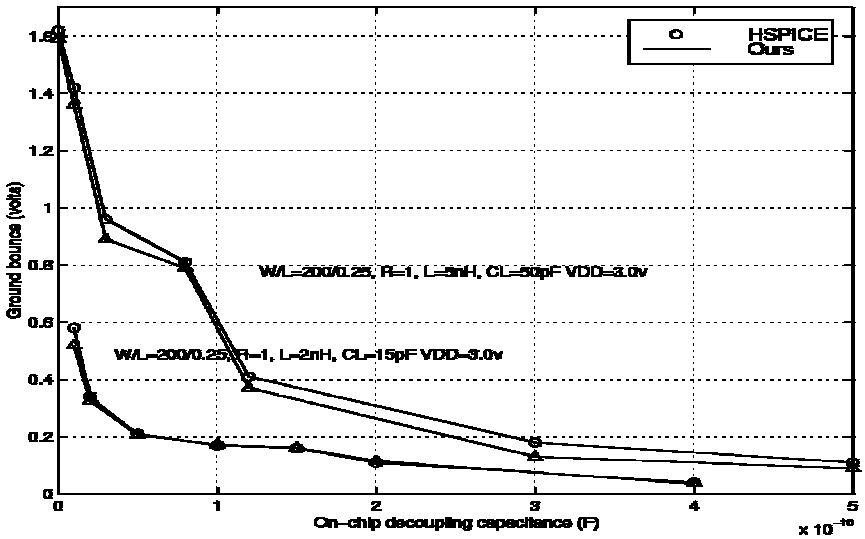
Differential –mode circuit



Common–mode circuit

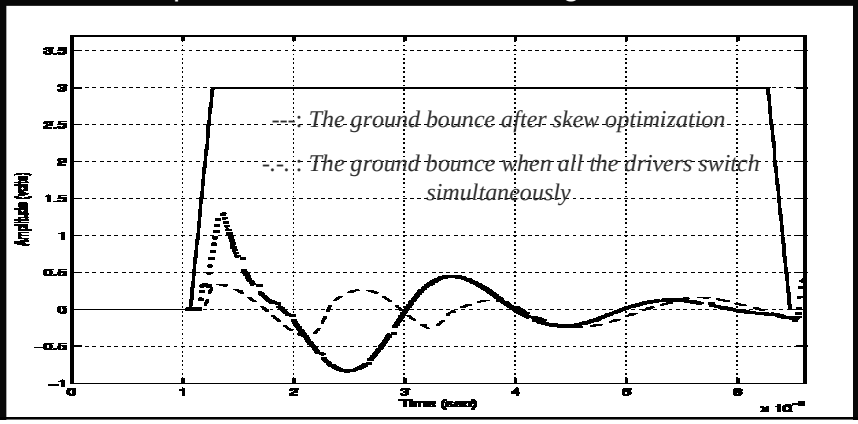
1. Decompose the circuit model into two distinct parts:
   - *1.a.* One part used for analysis of the differential-mode component of noise
   - *1.b.* The other part used for analysis of the common-mode component of noise.
2. Analyze the differential-mode circuit and compute the correct amount of the on-chip decoupling capacitor.

Simulation Results

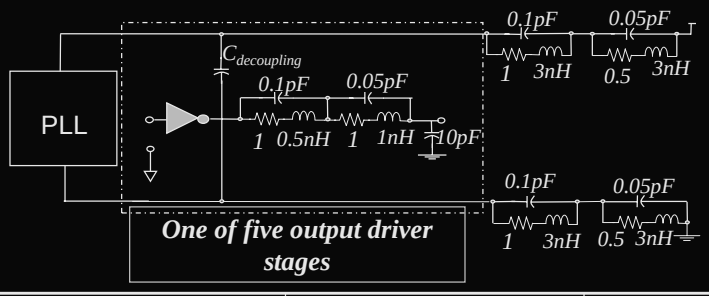


Skew Control

- To reduce the peak ground bounce delay the switching time of the output buffers
- Tune the switching time of the next driver to occur at the undershoot point of the current switching driver



Experimental Setup



Frequency offset (kHz)	Phase noise [dB/Hz] Analytical	Simulation [dB/Hz]
5.3	-92.2	-93.4
9.1	-96.4	-97.5
15.7	-100.3	-103
32.3	-109.3	-111.2
40	-110	-111.4
64	-112.4	-114.3
80	-115.6	-116.2
100	-119.7	-121.8

Conclusions

- A detailed analysis and optimization of the ground bounce was presented
- The method uses the accurate and simple chip-package interface circuit models
- The effect of ground bounce on the tapered buffer design was studied
- The effect of on-chip decoupling capacitor was analytically investigated
- A new skew control method for ground ounce optimization was proposed