Impact of Technology and Voltage Scaling on LEON3 Processor Performance and Energy

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I. Introduction

Although CMOS technology scaling has proceeded to sub-20nm nodes, FinFET devices are considered as the technology-of-choice for sub-20nm technology nodes due to the improved gate control [1]. On the other hand, voltage scaling provides us an energy efficient solution to the VLSI design, such as the near-threshold computing technique [2]. This work investigates the performance and energy consumption of LEON3 processor under technology and voltage scaling. Specifically, in order to study the impact of technology and voltage scaling, this work (i) develops 7nm gate length FinFET, ITRS 7nm FinFET (with 11nm actual gate length), ITRS 16nm CMOS, and ITRS 22nm CMOS Verilog-A device models using Synopsys TCAD tools [3], (ii) builds up the standard cell libraries using the developed Verilog-A models for the four previously mentioned technology nodes under a set of different supply voltage levels (i.e., from near-threshold to super-threshold), and (iii) synthesizes LEON3 processor (datapath plus L1 and L2 caches) using the developed standard cell libraries to compare the impact of technology and voltage scaling on the performance and energy consumption of LEON3 processor.

II. Cross-Layer Design and Simulation Flow

To investigate the impact of technology and voltage scaling, we employ a cross-layer design and simulation flow (Fig. 1), i.e., from device modeling to whole system synthesis.

A. Verilog-A Device Models for Different Technology Nodes

Table I shows the technology nodes investigated in this work to represent the technology scaling from the year of 2013 to the year of 2022. We develop the Verilog-A device models for the four technology nodes in Table I using Synopsys TCAD tools [3], and the physical dimensions and nominal voltage for each technology node are demonstrated in Table II. In particular, we use design parameters from ITRS [4] to build device models for ITRS 22nm CMOS, ITRS 16nm CMOS, and ITRS 7nm FinFET (with 11nm actual gate length), and 7nm gate length FinFET device models are designed in our previous work [5] with the 2-D model shown in Fig. 2. The device models are simulated by Synopsys TCAD to extract Hspice-compatible Verilog-A device models.

B. Standard Cell Library Construction

Based on Verilog-A device models for different technology nodes, we run Hspice simulations to build up standard cell libraries in an industrial standard format, i.e., Liberty library format (.lib). In a standard cell library, each logic cell, either combinational or sequential, is characterized with timing and power parameters under specific technology node and supply voltage. Table III shows the types of logic cells in each standard cell library, and there are also different sizings for each type of logic cell. Table IV summarizes all the fifteen standard cell libraries we have constructed for different technology nodes under different supply voltage levels (from near-threshold to super-threshold regions).

C. LEON3 Processor Synthesis

With the standard cell libraries constructed, we synthesize LEON3 processor with Synopsys Design Compiler. We use modified version of CACTI [6], a widely-used cache modeling tool, to characterize the L1 and L2 caches. We obtain the performance (operating frequency) and energy consumption per operation of LEON3 processor (datapath plus L1 and L2 caches) for different technology nodes under different supply voltage levels. The operating frequency is the maximum achievable frequency at the given technology node and supply voltage, whereas energy per operation is calculated as the ratio of the average power consumption over all instructions (accounting for both dynamic and leakage power consumptions) divided by the specified operating frequency.

III. Results and Discussion

The impact of voltage scaling on reducing the power and energy per operation can be seen in Fig. 3 and Fig. 4(b), respectively, which come at the cost of performance degradation (Fig. 4(a)). Voltage scaling is more significant in older bulk CMOS technologies because of (i) the higher contribution of the dynamic power (which has a cubic dependence on voltage) to the total power in older technologies, and (ii) the higher DIBL effect in bulk CMOS transistor. However, by employing optimized FinFET devices, performance improvement and energy reduction is still achievable in advanced technology nodes.

IV. Conclusion

Highly optimized FinFET devices are necessary for enabling aggressive voltage scaling, and hence improving the energy efficiency in advanced technology nodes. On the other hand, near-threshold operation is still a useful solution for energy minimization in FinFET-based circuits.

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References

[1] S. Sinha, et al., *Proc. DAC*, 2012. [2] H. Kaul, et al., *Proc. DAC*, 2012. [3] http://www.synopsys.com/tools/tcad. [4] http://www.itrs.net. [5] S. Chen, et al., *Proc. S3S*, 2014. [6] http://www.hpl.hp.com/research/cacti.

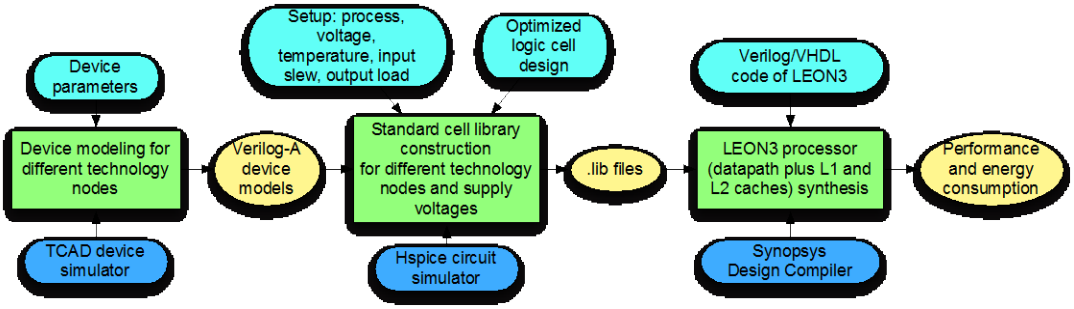

Fig. 1. Cross-layer design and simulation flow used in this work. The three main steps are: (i) device modeling for different technology nodes, (ii) standard cell library construction for different technology nodes and supply voltages, and (iii) LEON3 processor (datapath plus L1 and L2 caches) synthesis.

Table I. Technology nodes investigated in this work representing the technology scaling from the year of 2013 to the year of 2022.

Tech. Node (nm)	(Expected) Year of Introduction
ITRS 22nm CMOS	2013
ITRS 16nm CMOS	State-of-the-art
11nm gate length FinFET (ITRS 7nm)	2018
7nm gate length FinFET (Physical 7nm)	2022

Table II. Physical dimensions and nominal voltages of the technology nodes investigated in this work, namely, ITRS 22nm CMOS, ITRS 16nm CMOS, 11nm gate length FinFET (ITRS 7nm FinFET), and 7nm gate length FinFET devices.

	Channel length	Oxide thickness	Nominal voltage
ITRS 22nm CMOS	25nm	3.2nm	0.9V
ITRS 16nm CMOS	20nm	2.56nm	0.8V

	Gate length	Channel length	Fin thickness	Fin Height	Nominal voltage
11nm gate length FinFET (ITRS 7nm FinFET)	11.1nm	13.9nm	4.4nm	17.6nm	0.7V
7nm gate length FinFET	7.06nm	10.3nm	3.8nm	14nm	0.5V

Table III. Types of logic cells (combinational and sequential) in each standard cell library.

Combinational Logic Cells	Sequential Logic Cells
INV, NAND2, NAND3, NOR2, NOR3, XOR2, XNOR2	LATCH, DFF, DFFSR

Table IV. Fifteen standard cell libraries constructed for different technology nodes under different supply voltages.

Tech. Node	Supply Voltage (V)			
ITRS 22nm CMOS	0.5	0.6	0.7	0.8
ITRS 16nm CMOS	0.5	0.6	0.7	0.8
11nm gate length FinFET (ITRS 7nm FinFET)	0.4	0.5	0.6	0.7
7nm gate length FinFET (Physical 7nm FinFET)	0.3	0.4	0.5	

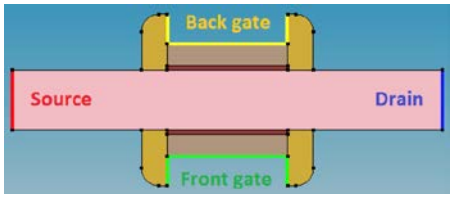

Fig. 2. 2-D model for 7nm gate length FinFET in TCAD device simulator.

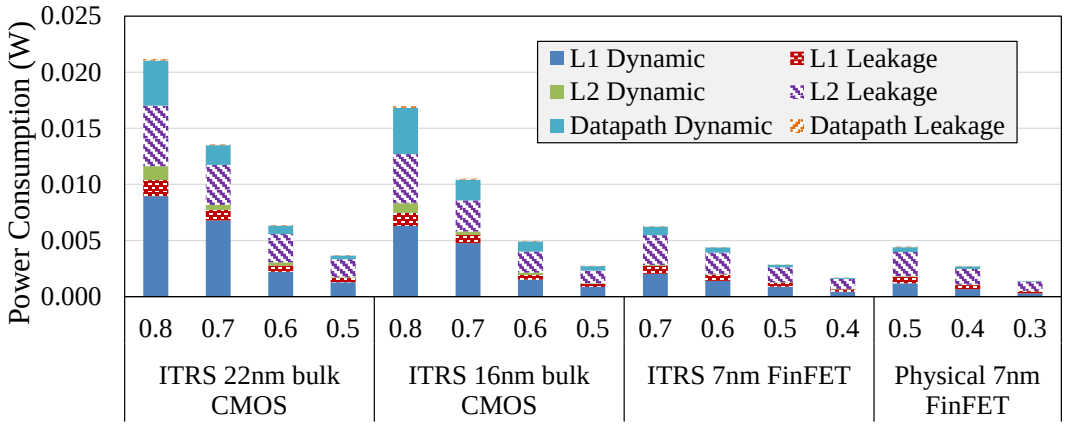

Fig. 3. Power breakdown of the LEON3 processor under different technology nodes and supply voltage levels. L1 is a 32KB, 2-way set-associative cache memory, whereas L2 is a 256KB, 4-way set-associative, 2-bank cache memory. As can be seen, leakage power becomes the dominant component of the total power consumption in deeply-scaled technologies.

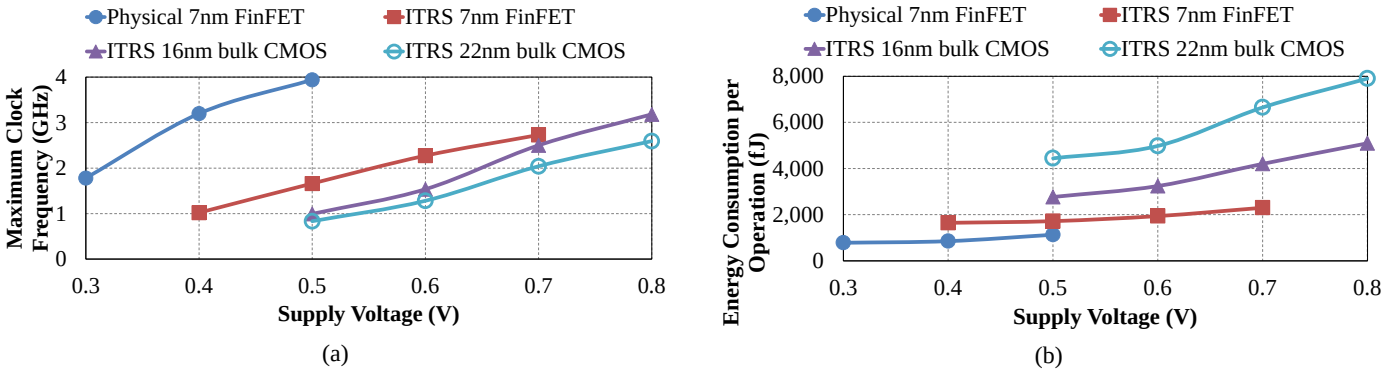

Fig. 4. The impact of technology and voltage scaling on (a) maximum clock frequency, and (b) energy consumption per operation of LEON3.