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Statistical Estimation of Leakage Power Dissipation in Nano-Scale CMOS Digital Circuits using Generalized Extreme Value Distribution

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Abstract—In this paper, we present an accurate approach for the estimation of statistical distribution of leakage power consumption in the presence of process variations in nano-scale CMOS technologies. The technique, which is additive with respect to the individual gate leakage values, employs Generalized Extreme Value (GEV) distribution. Compared to the previous methods based on (two-parameter) lognormal distribution, this method uses GEV distribution with three parameters to increase the accuracy. Using the suggested distribution, the leakage yield of circuits may be modeled. The accuracy of the approach is studied by comparing its results with those of a previous technique and HSPICE-based Monte Carlo simulations on ISCAS85 benchmark circuits for 45 nm CMOS technology. The comparison reveals a higher accuracy for the proposed approach. The proposed distribution does not add to the complexity and cost of simulations compared to the case of the lognormal distribution.

Index Terms— Manufacturing process variation, statistical leakage, GEV distribution.

1. INTRODUCTION

Process variations have had a large impact on the design of nano-scale digital integrated circuits. Process variations, which are created during the fabrication processes, such as photolithography and ion implantations, may be categorized into global (inter-die) versus local (intra-die) variations, and further subdivided into systematic and random variations [1]. Inter-die variations lead to different characteristics for the same device across different dies. Intra-die variations are responsible for variations in characteristics of the device within a single chip. Furthermore, some variations (mainly lithographical and layout-dependent ones) exhibit significant systematic spatial correlations while others, such as channel doping concentration and surface roughness, are random [1].

The leakage power dissipation, which increases with device scaling, has a strong dependence on the aforementioned variations. Two main components that induce the leakage power consumption include subthreshold and gate-leakage currents [2]. The subthreshold current has a strong (exponential) dependence on the channel length (L) and channel-length-independent threshold voltage (V_{th}) [3]. The large variability of these parameters in the presence of the process variations, leads to a considerable variation of leakage. The variation, which strongly influences the (leakage) yield of the circuit, should be modeled using statistical techniques for analysis and design optimization purposes. The statistical modeling of leakage currents and the (leakage) yield estimation have been a topic of many ongoing research efforts as reported in several publications (see, e.g., [4] and [5]).

An ideal statistical power modeling technique should be accurate, fast, and incremental (one simple addition per gate). The last requirement makes the technique computationally efficient for even for large circuits. There have been some approaches that are capable of producing acceptable results without requiring full-chip simulations [6]-[9]. These approaches, which estimated the leakage power variations, required complicated manipulations of their input parameters. Since the parameter manipulations were complex and interdependent, the approaches were not incremental [10]. Even an O(N) non-incremental algorithm would still be costly [10]. Even an O(N) (O(N) indicates the order of growth of computation cost (time) as a function of N where N is the number of logic cells in a chip.) non-incremental algorithm would still be costly [10]. .

There are a few works that rely on the summation of distributions (as a special case of incremental technique) for the statistical power analysis (see, e.g., [7]-[8]). These methods rely on the Wilkinson's approach for the addition of lognormal distributions. In this approach, the sum of lognormal distributions is approximated by another lognormal distribution whose parameters are found by moment matching. Thus, this approach is not directly additive, which means that the final lognormal

distribution cannot be obtained by simply adding two or more lognormal distributions [10]. While this approach finds accurate solutions for small chips relatively fast, any model that is primarily dependent on the Wilkinson's approach (O(N^2)) will not be scalable to large chips [10]. There are works like [11], which are both incremental and linear. In this work, the leakage variation is modeled as a set of orthogonal polynomials that can be added directly (linearly). While this method is incremental, it requires a different set of orthogonal polynomials for different distributions of variation sources [10].

To achieve the additive property with respect to some distributions for the total leakage current estimation, in [10], the leakage current is expressed by a polynomial function instead of an exponential one. It is shown that, in order to recalculate the chip leakage variation after changing some circuit elements, the computational complexity of their approach did not depend on the number of circuit element types (i.e., the size of a standard cell library) [10]. In case of the Wilkinson's approach, the complexity linearly depends on the number of the circuit element types. Similar to the Wilkinson's approach, reference [10] invokes a lognormal distribution to model the variation of the leakage power. To obtain the two parameters of the lognormal distributions, the first and second moments of the polynomial function of variation sources are invoked.

In an earlier work[1], we discussed that the accuracy of lognormal distribution for chip leakage may be improved by using another type of distribution. We considered more than 60 different distributions for the chip leakage power estimation and selected the best distribution among them which was generalized extreme value (GEV) distribution. By extending the Wilkinson method and calculating the third moment of chip leakage we calculated the three parameters of the GEV distribution. Although our proposed model increased the accuracy, it had one setback which was the requirement of calculating the third moment of the leakage. This increased the

computational complexity from O(N2) in Wilkinson's approach to O(N3). In this paper, we kept the accuracy obtained by the GEV distribution yet improved the computational complexity. This is achieved by using an additive method to calculate the distribution parameters and eliminating the need for calculating the third moment. Compared with the traditional Wilkinson's approach, the proposed approach provides more than four times improvement in the computation time for the ISCAS85 benchmark circuits and five times enhancement in the accuracy of a 99 percentile point of the leakage cumulative distribution function (CDF).

The rest of the paper is organized as follows. In Section 2, we investigate the accuracy of different distributions for fitting the leakage variations. Section 3 describes the approach used to find the three parameters of the proposed leakage distribution function. Section 4 discusses the results, and finally, Section 5 concludes the paper.

2. FITTING LEAKAGE POWER VARIATION BY GENERALIZED EXTREME VALUE DISTRIBUTION

In this section, to improve the accuracy of leakage power analysis, we present an alternative statistical distribution function to capture the variations of the leakage power. The main motivation to provide a new statistical distribution function is that in nano-scale technologies, the distribution of the leakage variation for some states of a (CMOS) logic gate may deviate from the lognormal function. Note that a state refers to the combination of Boolean signal values applied to the inputs of the gate in question. The leakage variations for different states of a simple 2-Input NAND gate in a 45 nm CMOS technology obtained using HSPICE Monte Carlo (MC) simulations are shown in Fig. 1. As the results reveal, the lognormal distribution does not accurately model the variations for some states. One may thus expect that the leakage variation of a complex circuit with a large number of constituent logic gates can sharply deviate from the lognormal distribution. This inspired us to look for a different distribution function for more accurate modeling of the statistical variation of

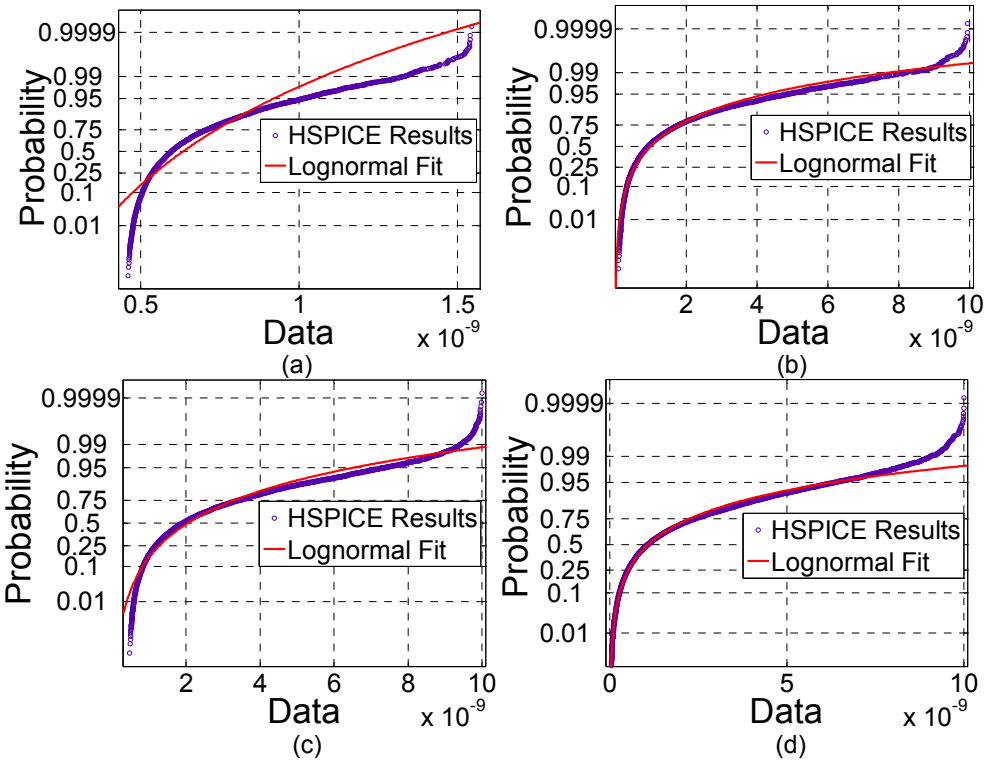

Fig. 1 Probability plot of leakage power distribution of a 2-Input NAND gate in states (a) 00 (b) 01 (c) 10 (d) 11. All simulations have been performed in 45 nm technology.

the leakage power. First, we performed Monte-Carlo (MC) simulations for the ISCAS85 benchmark circuits [12]. Then, using MATLAB, we fitted the leakage variations by different distribution functions [12]. The goodness-of-fit values for different distribution functions were assessed using the chi-squared test [13]. For example, for the leakage distribution of the c1355 circuit, five best distributions included Generalized Extreme Value (a three parameter distribution, or 3P for short), Frechet (3P), Pearson5 (3P), Burr5 (3P), and Log-Logistic (3P), respectively. The Lognormal (2P) distribution, which is used by previous works, ranked 14th. Therefore, we propose the GEV distribution function as a more accurate distribution function for capturing leakage power variations. The GEV distribution function has three parameters, and consequently, has one more degree of freedom compared to the lognormal distribution, which relies on two parameters.

As an example, Figure 2 compares the accuracies of the GEV and lognormal distributions in modeling the Probability Density Function (PDF) of leakage variations for c2670 (medium size circuits) and c7552 (the largest circuit) in the ISCAS benchmark suite. As is evident from the figure, GEV models the variation more accurately especially around the peak and toward the right tail of the distribution. The PDF of GEV distribution is given by [13]

$$f(x|\mu,\sigma,\xi)=\frac{1}{\sigma}t(x)^{\xi+1}e^{-t(x)} \quad , \quad t(x)=\begin{cases}\left(1+\xi\left(\dfrac{x-\mu}{\sigma}\right)\right)^{-1/\xi} & \text{if } \xi\neq 0\\ e^{-(x-\mu)/\sigma} & \text{if } \xi=0\end{cases} \tag{1}$$

where μ, σ, and ξ are, respectively, location, scale, and shape parameters of the distribution.

After finding a more accurate distribution function for the leakage variation, next, we need to calculate the parameters of the distribution. In the next section, we discuss an analytical method for calculating the GEV distribution parameters using an additive model.

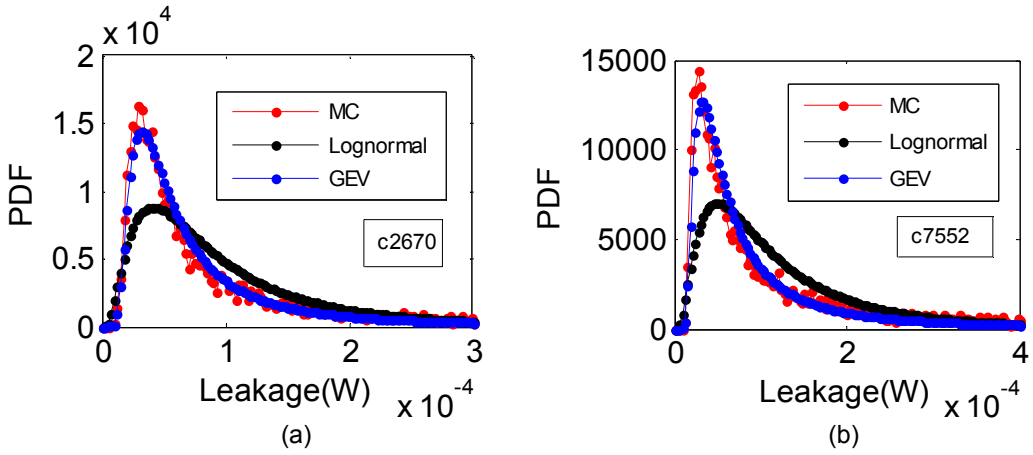

Fig. 2. Comparison between PDF of GEV and Lognormal distributions for (a) c2670 and (b) c7552 circuits.

3. ADDITIVE LEAKAGE POWER MODEL FOR FINDING PARAMETERS OF GENERALIZED EXTREME VALUE DISTRIBUTION

Most models for the statistical leakage analysis in a VLSI circuit use an exponential functional form to capture the dependence of logic gate leakage current on the threshold voltage (and indirectly channel length), which makes the inclusion of additional logic gates in the circuit an intricate task (because the addition of two exponential functions does not lead to another exponential function).

A. Additive Leakage Power Model

In the additive leakage power model, the leakage current (power) is expressed using a polynomial functional form instead of an exponential one [10]. The polynomial function may be obtained from the series expansion of the exponential relation, and hence, the inclusion of higher-order terms provides higher accuracy at the expense of increasing the computational cost. The polynomial relation is a function of variation sources such as the threshold voltage and channel length. In [10], the leakage power is approximated by a fourth-order polynomial of variation sources as

$$P = P_0.(a_0 + \sum_{1\le i<j\le n}(b_{ij1}X_iX_j + b_{ij2}X_i^2X_j^2) + \sum_{1\le i<n}(a_{i1}X_i + a_{i2}X_i^2 + a_{i3}X_i^3 + a_{i4}X_i^4) \quad (2)$$

where $X = (X_1, X_2, \ldots, X_n)$ is the vector of the variation sources and a_{ik}, b_{ijk}, and a_0 are the coefficients obtained by curve fitting through HSPICE simulations. There are totally n^2+3n+1 terms in the polynomial, where n is the number of variation sources. Using the polynomial leakage power model, the chip leakage power may be calculated as the sum of leakage powers of all circuit elements [10]:

$$P_{chip} = \sum_{i \in T} N_i P_i \tag{3}$$

Here, T denotes the set of circuit element types (with the size of N_t) and N_i is the number of circuit elements of type i. Since the leakage powers of all circuit elements are expressed in a polynomial form as in (2), it is easy to see that P_{chip} is also in the same functional form. Then, the distribution of the chip leakage power, may be approximated using a lognormal random variable as [14]

$$P \approx P_0 e^{R_N} \tag{4}$$

The PDF of the lognormal distribution is given by

$$g(x|\mu,\sigma) = \frac{1}{x\sqrt{2\pi\sigma^2}} e^{-\frac{(\ln x-\mu)^2}{2\sigma^2}} \tag{5}$$

where R_N is a Gaussian random variable. The mean of the leakage power is obtained from [10]

$$\mu_p = E[P] = P_0\left(a_0 + \sum_{1\le i<j\le n} b_{ij2} + \sum_{1\le i\le n}\left(a_{i2} + a_{i3}m_{i3} + a_{i4}m_{i4}\right)\right) \tag{6}$$

Also, by calculating the second moment as [10]

$$\begin{aligned} m_{2p} &= E[P^2] \\ &= P_0\{a_0^2 + \sum_{1\le i\le n}(2a_0a_{i2} + 2a_0a_{i3}m_{i3} + 2a_0a_{i4}m_{i4} + a_{i1}^2 + a_{i2}^2m_{i4} + a_{i3}^2m_{i6} + a_{i4}^2m_{i8} \\ &+ 2a_{i1}a_{i2}m_{i3} + 2a_{i1}a_{i3}m_{i4} + 2a_{i1}a_{i4}m_{i5} + 2a_{i2}a_{i3}m_{i5} + 2a_{i2}a_{i4}m_{i6} + 2a_{i3}a_{i4}m_{i7}) \\ &+ \sum_{1\le i<j\le n}(2a_0b_{ij2} + b_{ij1}^2 + b_{ij2}^2m_{i4}m_{j4} + 2b_{ij1}b_{ij2}m_{i3}m_{j3} + 2a_{i2}a_{j2} + 2a_{i2}a_{j3}m_{i2}m_{j3} \\ &+ 2a_{i2}a_{j4}m_{i2}m_{j4} + 2a_{i3}a_{j4}m_{i3}m_{j4})\} \end{aligned} \tag{7}$$

the variance is calculated from

$$\sigma_P^2 = m_{2P} - \mu_P^2 \tag{8}$$

Here, m_{ik} is the k^{th}-order moment for the i^{th} variation source (X_i). The parameters (μ,σ) of $g(x|\mu,\sigma)$ are obtained from [14]

$$\mu = \ln\left(\mu_P^2 / \sqrt{\sigma_P^2 + \mu_P^2}\right) \text{ and } \sigma = \sqrt{\log\left(\frac{\sigma_P^2}{\mu_P^2} + 1\right)} \tag{9}$$

Next, we show the procedure for obtaining the parameters of the GEV distribution function using the additive approach.

B. Parameter Extraction for the GEV Distribution

As discussed previously, in order to fit leakage variation by a lognormal distribution, the first and second moments should be calculated. Since the calculation of the second moment depends on the number of gates (see (7)), this calculation may increase the simulation time too much when the number of gates increases. The situation becomes worse in the case of calculating the third moment. To fit the leakage variation by a lognormal distribution, we have to solve a system of two equations and two unknowns (8) to find the parameters of the lognormal distribution. The GEV distribution function has three parameters which may be obtained from a system of three equations and three unknowns. In [10], the system of two equations and two unknowns was obtained by matching the first and second moments. As explained previously, matching the third moment is practically infeasible due to the large number of polynomials. As a result, we should form the system of three equations and three unknowns for GEV by a different solution. For the first two equations, we follow the method presented by [10] where (8) is used. Using these equations, we equate the mean and variance of the GEV distribution to the right-hand sides of (8), respectively. The mean of GEV distribution is obtained from [13]

$$Mean = \begin{cases} \mu + \sigma \dfrac{\Gamma(1-\xi)-1}{\xi} & \text{if } \xi \neq 0, \xi < 1, \\ \mu + \sigma\gamma & \text{if } \xi = 0, \\ \infty & \text{if } \xi \geq 1, \end{cases} \tag{10}$$

where γ is Euler's constant. Also, the variance of GEV distribution is given by [13]

$$Variance = \begin{cases} \sigma^2 (g_2 - g_1^2)/\xi^2 & \text{if } \xi \neq 0, \xi < 1/2, \\ \sigma^2 \dfrac{\pi^2}{6} & \text{if } \xi = 0, \\ \infty & \text{if } \xi \geq 1/2, \end{cases} \tag{11}$$

where $g_k = \Gamma(1 - k\xi)$ for k = 1 and 2.

Now, in order to form the third equation, we assume that the lognormal distribution accurately estimates the maximum likelihood point. Using this assumption, we can find this point for the lognormal distribution and find the GEV distribution parameters such that the maximum likelihood for the GEV distribution occurs at the same point. To demonstrate the motivation for this assumption, in Fig. 3, we have plotted the histogram of the leakage variations obtained from the simulations as well as the fitted lognormal and GEV distributions for the c7552 circuit.

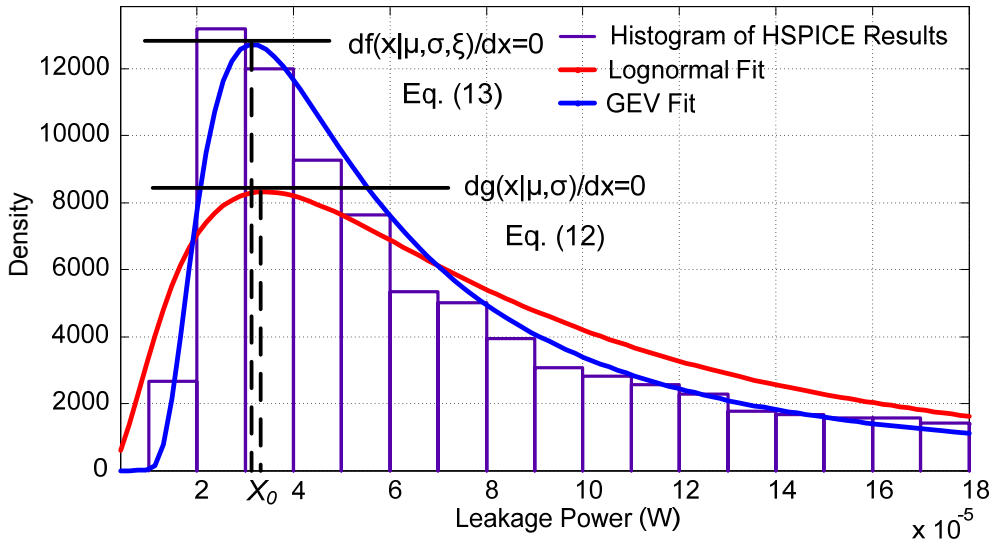

Fig. 3 Histogram of simulation, lognormal fit, and GEV fit of C7552 circuit in 45 nm technology.

The figure shows that the maximum likelihood points obtained from the GEV and lognormal distributions are very close to each other. At the point of the maximum likelihood, the derivative of the lognormal distribution function is equal to zero.

By setting the derivative of (5) to zero, one obtains the maximum point as

$$\frac{\partial g(x|\mu,\sigma)}{\partial x}\Big|_{x=x_0} = 0 \qquad , x_0 = e^{\mu-\sigma^2} \tag{12}$$

Similarly, the maximum point for the GEV distribution is obtained from

$$\frac{\partial f(x|\mu,\sigma,\xi)}{\partial x}\Big|_{x=x_0} = 0 \ , x_0 = \begin{cases} \mu + \sigma\dfrac{(1+\xi)^{-\xi}-1}{\xi} & \text{if } \xi \neq 0 \\ \mu & \text{if } \xi = 0 \end{cases} \tag{13}$$

By setting these two maximum points equal, the third equation is obtained. Using this system of equations, all three parameters of the GEV distribution function may be obtained.

Note that, compared to [10], we have only added (13). Since, we just solve a simple equation which is independent of the number of cells or complexity of circuit, the proposed method is as efficient as the method presented in [10]. In the next section, we compare the results of our technique with those of [10].

4. SIMULATION RESULTS AND COMPARISON

The accuracies of the proposed approach based on the GEV distribution and the lognormal distribution fitting were investigated using the ISCAS85 benchmark circuits. For the simulations, we used the 45nm CMOS technology of Nangate open cell library [15]. The variation sources considered were NMOS transistor threshold voltage (V_{thn}), PMOS transistor threshold voltage (V_{thp}), and effective channel length (L_{eff}), respectively. We performed 10,000 Monte Carlo simulations on the circuits. For L_{eff}, we assumed a Gaussian distribution. For the 3σ channel length variations, we considered the inter-die and intra-die components to be, respectively, 8% and 6% (see, e.g., [10]). For the intra-die variations of the channel length, we partitioned the entire circuit into N squares and assumed that the correlation coefficient between

each two squares was inversely proportional to their distance. For the benchmark circuits in Table 1, we took N = 4. For the gate-length independent threshold voltages (V_{thn0} and V_{thp0}), we considered only random variations with 3σ value equal to 20% of the nominal values. This randomness in the threshold voltage variations is due to the random dopant fluctuation phenomenon which is the dominant component in the threshold voltage variation [16].

The CDF is used to obtain the leakage yield of the circuit (chip). Figure 4 (a,b) compares the CDF of these two distributions with the results of the Monte Carlo simulation for the c2670 and c7552 circuits. As the comparison in Figure 4 (c,d) clearly shows, at high values of CDF, which are used for the yield estimation, the GEV distribution is more accurate than the lognormal distribution. In Table 1, we have reported the percentile errors of the GEV and lognormal distribution functions compared to the Monte Carlo simulation for the ISCAS85 benchmark circuits. As the results reveal, for GEV, the average errors for 90%, 95%, and 99% percentile points were 0.2%, 0.3%, and 2.0%, respectively. For the case of lognormal, the errors were 15.1%, 16.3%, and 11.0%, respectively. This verifies a higher accuracy for the GEV distribution function. As mentioned before, this improvement in the accuracy has been achieved at almost no computational cost.

Table 1 90%, 95%, and 99% Percentile-Point Error Comparison between GEV and Lognormal Distribution Functions.

Bench mark	Our Method			Lognormal Approximation			Monte Carlo		
	90% (μW)	95% (μW)	99% (μW)	90% (μW)	95% (μW)	99% (μW)	90% (μW)	95% (μW)	99% (μW)
C17	0.543 (0.3%)	0.823 (0.4%)	1.30 (2.6%)	0.459 (-15.3%)	0.662 (-19.2%)	1.41 (11.0%)	0.542	0.820	1.27
C432	29.1(0.0%)	42.9 (0.1%)	62.9 (1.5%)	24.3 (-16.4%)	34.4 (-19.6%)	67.0 (7.8%)	29.1	42.8	62.1
C499	38.7 (0.2%)	50.4 (0.4%)	67.3 (3.1%)	33.0 (-14.5%)	44.6 (-11.1%)	78.4 (16.7%)	38.6	50.2	65.3
C880	40.4(0.1%)	54.2(0.5%)	79.5(3.4%)	86.4(-15.3%)	53.3(-12.1%)	87.7(14.1%)	40.3	53.9	76.9
C1355	42.2 (0.4%)	61.1 (0.7%)	92.7 (2.7%)	35.1 (-16.6%)	50.1 (-17.4%)	96.8 (7.1%)	42.1	60.7	90.3
C1908	77.1 (0.5%)	106 (0.2%)	141 (1.8%)	66.2 (-13.8%)	90.3 (-16.2%)	164 (15.2%)	76.8	105	139
C2670	237 (0.4%)	327 (0.3%)	465 (2.1%)	208 (-11.8%)	281.1 (-16.0%)	497 (8.2%)	236	326	456
C5315	277(0.4%)	365.7(0.2%)	487(1.1%)	238.5(-13.6%)	301.9(-17.3%)	526.8(9.3%)	276	365	482
C6288	302.3(0.1%)	397.4(0.1%)	531(1.7%)	246.4(-18.4%)	319.9(-19.4%)	558.6(6.8%)	302	397	523
C7552	317 (0.1%)	433(0.5%)	570 (2.0%)	267 (-15.7%)	364.2 (-15.5%)	654 (14.5%)	317	431	559
Ave	0.2%	0.3%	2.0%	-15.1%	-16.3%	11.0%	-	-	-

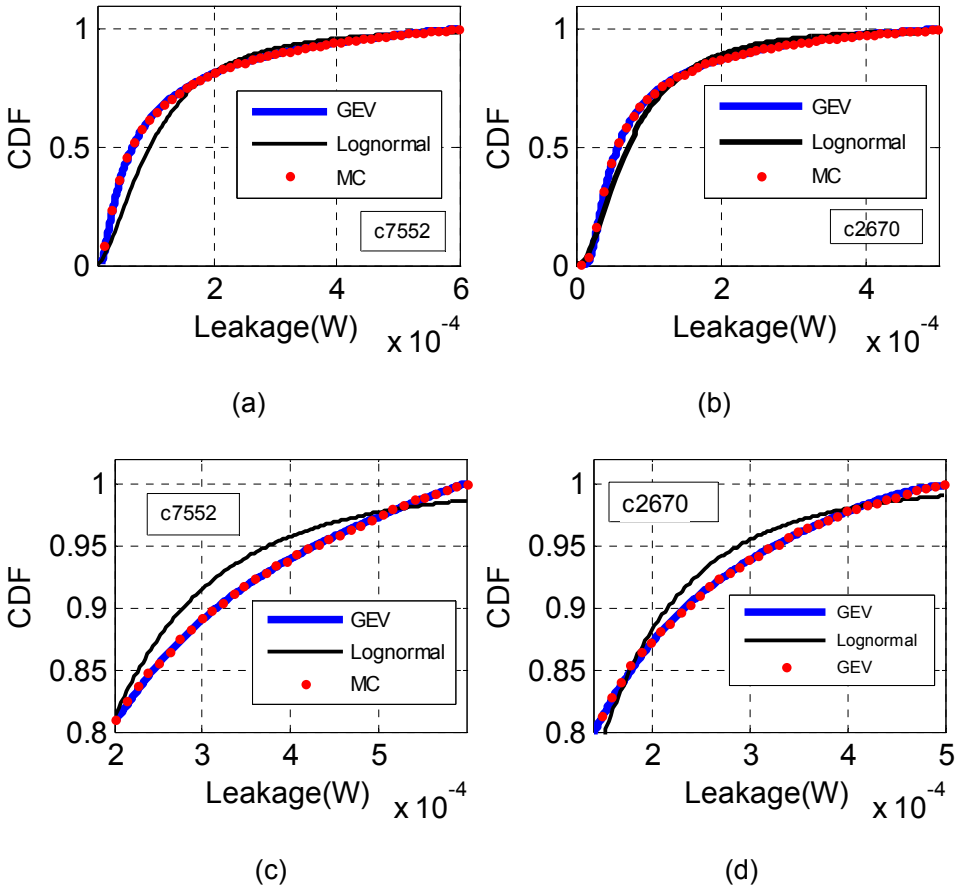

Fig. 4 Comparison between CDFs of GEV and Lognormal distributions for c7552 and c2670 in the (a,b) whole range and (c,d) for leakage larger than 2 μW.

5. CONCLUSION

In this work, we proposed the GEV distribution function as an alternative to the lognormal distribution function for modeling the chip leakage power variation of nano-scale CMOS digital circuits under process variations. The GEV distribution function has one more parameter compared to the lognormal distribution function. The three parameters were calculated using a system of three equations/unknowns. Similar to a recently published work based on the lognormal distribution function, we used the additive technique to obtain two equations which expressed the equalities of the means and variances of the distributions. To obtain the third equation, we suggested matching the point that the maximum likelihood of the distribution occurred. The added computational cost was negligible compared to that of the lognormal distribution. We verified the accuracy of our method on the ISCAS85 benchmark

circuits in a 45 nm CMOS technology under variations of NMOS and PMOS transistor threshold voltage and effective channel length. The simulation results showed that the approach estimated 90%, 95%, and 99% percentile points with average errors of 0.2%, 0.3%, and 2.0%, respectively. The errors were considerably lower than those of a recently proposed technique based on the lognormal distribution function.

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