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Statistical Functional Yield Estimation and Enhancement of CNFET-Based VLSI Circuits

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***Abstract*— Carbon nanotube field effect transistors (CNFETs) show great promise as extensions to silicon CMOS. However, imperfections, which are mainly related to carbon nanotubes (CNTs) growth process, result in metallic and nonuniform CNTs leading to significant functional yield reduction. This paper presents a comprehensive technique for statistical functional yield estimation and enhancement of CNFET-based VLSI circuits. Based on experimental data extracted from aligned CNTs, we propose a compact statistical model to estimate the failure probability of a CNFET. Using the proposed failure model, we show that enhancing the CNT synthesis process alone cannot achieve acceptable functional yield for upcoming CNFET-based VLSI circuits. We propose a technique which is based on replacing each transistor by series-parallel transistor structures to reduce the failure probability of CNFETs in the presence of metallic and nonuniform CNTs. The technique is adapted to use single directional independence, which is inherent in aligned CNTs, to enhance the functional yield as validated by theoretical analysis and simulation results. Tradeoffs between failure probability reduction and design overheads such as area and current drive are explored. As demonstrated by extensive simulation results, the proposed technique achieves 80% functional yield in CNFET technology at the cost of 7.5X area and 34% current drive overheads if the CNT density and the fraction of semiconducting CNTs are improved to 200 CNTs per μm and 99.99%, respectively.**

***Index Terms*— Carbon nanotube field effect transistor (CNFET), failure probability, statistical functional yield.**

I. Introduction

SILICON-BASED integrated circuit technology is approaching its physical limits in nano-scale era [1], [2]. Materials and nano-device researches continue to produce candidates for post silicon-era design [1]–[3]. Carbon nanotube field effect transistors (CNFETs), consisting of semiconducting single-walled carbon nanotubes (CNTs), show great promise as future integrated circuits in the post-silicon era [4]–[6]. Fig. 1 shows the side view of the device structure of a CNFET with ideal parallel semiconducting-CNTs (s-CNTs). The CNFET, which is a 1-D structure with a near-ballistic transport capability and high carrier mobilities (10^3–10^4 cm^2/V·s), can potentially offer excellent device characteristics and an order-of-magnitude better energy-delay product over standard CMOS devices [5], [6].

Unfortunately, the current CNT synthesis processes are far from ideal [7]. Depending on the chirality, a CNT can be either metallic or semiconducting [8], [9]. Current CNT growth techniques produce a mixture of metallic-CNTs (m-CNTs) and s-CNTs. A third of the CNTs are grown as metallic [8] creating source-drain short defects in the CNFETs. Hence, chemical techniques for m-CNT removal after growth, such as selective etching [9], are used to eliminate the m-CNTs. However, current m-CNT removal techniques are not perfect as they do not remove all m-CNTs and also inadvertently remove some useful s-CNTs. Another major limitation in CNT fabrication is the inability of growing perfectly aligned and uniformly distributed s-CNTs. Although advances in CNT synthesis have been achieved to improve the average density of CNTs from the value obtained today [10], [11], large variations are still present in the CNT density [12]. CNT density variations (nonuniform CNTs) in a typical CNT synthesis process lead to considerable deviations in the number of useful s-CNTs. Specifically, CNT density variations result in void CNFETs, i.e., CNFETs without any useful s-CNT, leading to open defects in CNFETs.

While recent research has addressed some issues of CNFET technology, one major challenge has yet to be investigated, i.e., high yield design of CNFET-based VLSI circuits in the presence of metallic and nonuniform CNTs. Recently, some aspects of CNT synthesis related to functional yield of CNFET circuits have been investigated.

In particular, Zhang *et al*. [12] present a parameterized model for CNT density variation to quantify the impact of density variations on design metrics such as noise margins and delay variations of CNFET circuits. In [13], Zhang *et al*. show that CNT density variation leads to void CNFETs resulting in circuit failures. Taking advantage of the spatial correlation observed in directional CNT growth, they enforce the CNFETs to be aligned with each other to reduce the failure probability at the chip-level. Reference [14] presents a probabilistic method to analyze the impacts of metallic tubes on static power and noise margins of CNFET circuits under chemical nonidealities. Ashraf *et al*. [15] present a structure of CNFETs that reduces the statistical probability of short defects between the source and drain of a transistor in the presence of metallic tubes. Patil *et al*. [16] present

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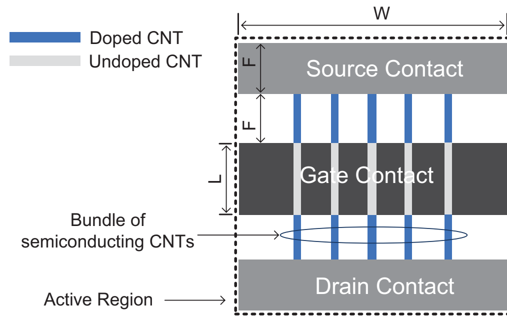

Fig. 1. Side view of an ideal CNFET with five s-CNTs in the active region. S-CNTs are grown on or transferred to a substrate using chemical synthesis. The regions of CNTs under the gate are undoped. The conductivity of these undoped regions is controlled by the gate. The source and drain regions of the CNTs are heavily doped. The gate, source, and drain contacts, and interconnects are defined by conventional lithography [4], [7]. W and L are the CNFET width and length, respectively. F is the lithographic half-pitch (minimum feature size).

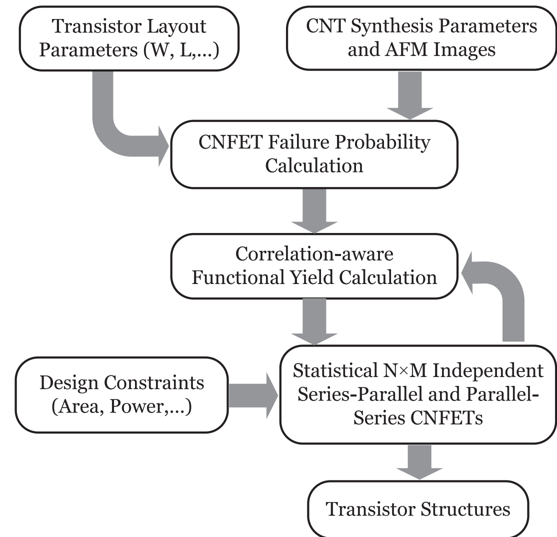

Fig. 2. Functional yield-aware CNFET-based circuit design flow.

a VLSI-compatible m-CNT removal technique called VMR, which can mitigate issues caused by existing m-CNTs. However, VMR results in more CNT density variations. Lately, a design technique called asymmetrically correlated CNTs (ACCNT) [17] has been proposed which uses correlated CNTs to achieve m-CNT tolerance that does not require any m-CNT removal of any kind. The proposed approach uses independent stacks of series CNFETs to tolerate short defects caused by m-CNTs, and meanwhile, takes advantage of CNT correlations in parallel branches of CNFETs to increase the device drive strength without degrading the defect tolerance. The method, however, does not support open defects caused by void CNFETs. Zarkesh–Ha *et al*. [18] show that the open defect is a critical issue in CNFET technology and perform a stochastic analysis to demonstrate that the CNT density variation imposes a crucial limitation on ACCNT technology. However, the failure model does not rely on extracted chemical synthesis data, which is necessary for any attempts to analyze or optimize designs statistically. In other words, ignoring parameter characterization in failure analysis may lead to significant error in statistical yield modeling.

To the best of our knowledge, there is no inclusive approach to analyze and improve the functional yield of CNFET technology considering CNT synthesis imperfections. In this paper, we present a comprehensive approach to functional yield estimation and enhancement of CNFET-based VLSI circuits.

The rest of this paper is organized as follows. Section II presents the proposed flow of functional yield-aware CNFET-based circuit design. Section III presents the statistical failure analysis of CNFETs, and then, investigates the impacts of synthesis process parameters on CNFET failure probability. Section IV presents different transistor-level redundancy structures, and also studies the impact of CNT correlation on failure probability. Section V proposes the ISP/IPS transistor structures for CNFET with support of theoretical analysis and simulation results. In Section VI, the design space is analyzed and extensive discussions are made on the results to derive advantageous design guidelines. Finally, Section VII concludes this paper.

II. Functional Yield-Aware CNFET-Based Circuit Design Methodology

As we move toward radical nanoelectronic devices, such as CNFETs, we anticipate less reliable devices. For instance, in comparison to the 10^{-9}–10^{-7} device failure rates in CMOS technology [27], the failure rates in emerging nanotechnologies are projected to be in the order of 10^{-2} due to the extremely small device sizes and intricacies of the fabrication process. It is, therefore, imperative to accept the fact that the underlying devices will no longer be perfect leading to considerable reduction in functional yield of the designs. Hence, it is necessary to enable the design of robust circuits that are resilient to process imperfections.

Implementing a resilient circuit using imperfect CNFET devices requires a failure-based transistor characterization and design optimization process that is fully integrated into the design flow. This paper proposes such a design methodology to help designers develop high-yield CNFET-based VLSI circuits. The proposed design flow, shown in Fig. 2, includes early-stage design steps, where the circuit designer is selecting a CNFET redundant structure based on the CNT synthesis fabrication parameters and design constraints such as area overheads.

Atomic force microscopy (AFM) images of grown CNTs are processed to extract the CNT spacing distribution, and then, open and short failure probabilities of CNFETs are approximated using rigorous probabilistic analysis. The compact CNFET failure probability is the primary mathematical model that can be used for chip-level yield analysis in the circuit design flow (it is notable that, calculating the CNFET failure probability experimentally can be time-consuming as this probability depends on the transistor width). Then, based on the proposed model and using the current CNT synthesis parameters, functional yield constraint of CNFET-based VLSI circuits is investigated.

To handle massive CNT synthesis imperfections without compromising functional yield, redundant structures at

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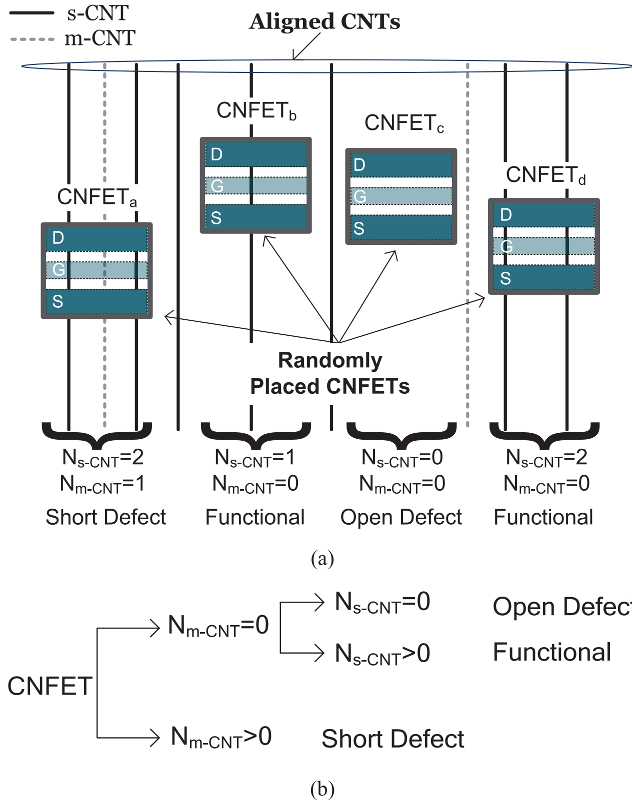

Fig. 3. (a) CNFETs randomly placed on aligned s- and m-CNTs. $N_{\text{m-CNT}}$ represents the number of m-CNT and $N_{\text{s-CNT}}$ expresses the number of s-CNT in a CNFET. CNFET_b and CNFET_d are functional where CNFET_a and CNFET_c have short and open defects, respectively. (b) Defect classification of CNFETs regarding to the number of m- and s-CNTs placed in the active region.

transistor level, e.g., series–parallel/parallel–series transistor structures are presented. The proposed structures are based on the single directional independence that is intrinsic to CNFETs, i.e., independence which is uniform only in one orientation. The proposed structures provide satisfactory immunity toward metallic and nonuniform CNTs at the same time, which was ignored in [17]. The transistor-level redundancy can be easily incorporated into the CNFET failure model to compute the yield of circuits with composite array of transistors.

Finally, the designer can pick one of the CNFET-based redundant structures based on the design constraints, such as area overhead and current drive, and the targeted functional yield.

III. Statistical Failure Analysis of CNFET

Unlike the standard CMOS process, where each mask layer is precisely aligned, the process of CNT growth always results in random and undetermined CNT placement.

Fig. 3(a) illustrates four randomly placed CNFETs located on aligned CNTs. Depending on the location of a CNFET, there is a random number of s- and m-CNTs ($N_{\text{m-CNT}}$ and $N_{\text{s-CNT}}$, respectively) under the CNFET active region, i.e., a region that encloses the CNFET. For instance, CNFET_a has two s-CNTs and one m-CNT. CNFET_b and CNFET_d have one and two s-CNT in the active region, respectively.

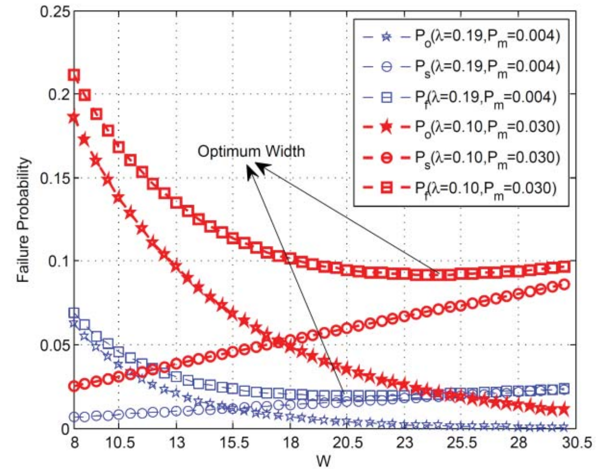

Fig. 4. Illustration of the total failure probability and its components, versus the CNFET widths in two synthesis processes.

CNFET_c does not contain any m- or s-CNT. We refer to a CNFET without any CNT as a "void CNFET" which results in an *open defect* (CNFET_c). Including at least one m-CNT in the active region of a CNFET leads to a source-drain short defect or briefly *short defect* (CNFET_a). A CNFET can be a "functional device" if it encounters neither open nor short defects (CNFET_b and CNFET_d). Based on the definitions, we classify a CNFET founded on the number of m- and s-CNT which is shown in Fig. 3(b). We denote the open and short failure probability of a CNFET by $P_{\text{O,CNF}}$ and $P_{\text{S,CNF}}$ respectively. A CNFET can be considered as *defective* if its expected behavior changes due to either an open or a short defect. So, the *total failure probability* of a CNFET, $P_{\text{F,CNF}}$, can be expressed as follows:

$$P_{\text{F,CNFET}} = P_{\text{O,CNFET}} + P_{\text{S,CNFET}}. \tag{1}$$

We use the measured CNT spacing data, i.e., the distance between neighboring CNTs and is denoted by S_{CNT}, to estimate the open and short failure probability of a CNFET (detailed derivation of CNFET failure probability is included in Appendix A).

The short and open failure probability of a CNFET with width W can be expressed as follows:

$$P_{\text{O,CNFET}} = e^{-\lambda_{S_{\text{CNT}}}{}^{W}} - W\lambda_{S_{\text{CNT}}}\left(\Gamma\left(0, W\lambda_{S_{\text{CNT}}}\right)\right) \tag{2}$$

$$P_{\text{S,CNFET}} = 1 - \left(e^{-\frac{\lambda_{S_{\text{CNT}}}}{P_m}W} - W\frac{\lambda_{S_{\text{CNT}}}}{P_m}\left(\Gamma\left(0, W\frac{\lambda_{S_{\text{CNT}}}}{P_m}\right)\right)\right) \tag{3}$$

where Γ is the incomplete gamma function [20], $\lambda_{S_{\text{CNT}}}$ is the statistical distribution parameters of CNT spacing and P_m is the probability of any CNT being an m-CNT.

Based on (1), (2), and (3), the statistical failure probability of a CNFET can be expressed by

$$P_{\text{F,CNFET}} = e^{-\lambda_{S_{\text{CNT}}}{}^{W}} - W\lambda_{S_{\text{CNT}}}\left(\Gamma\left(0, W\lambda_{S_{\text{CNT}}}\right)\right) + 1 - \left(e^{-\frac{\lambda_{S_{\text{CNT}}}}{P_m}W} - W\frac{\lambda_{S_{\text{CNT}}}}{P_m}\left(\Gamma\left(0, W\frac{\lambda_{S_{\text{CNT}}}}{P_m}\right)\right)\right). \tag{4}$$

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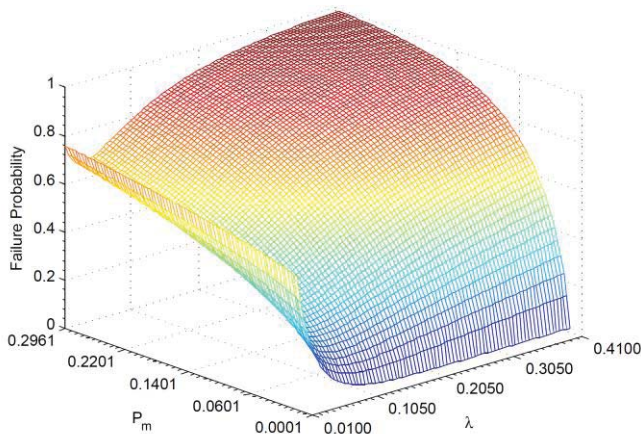


Fig. 5. Illustration of synthesis parameters impacts on total failure probability.

Using the proposed model, we analyze the failure probability of a CNFET in various CNT synthesis technologies. Fig. 4 illustrates the $P_{\text{F,CNFET}}$ and its components, $P_{\text{O,CNFET}}$ and $P_{\text{S,CNFET}}$, versus the CNFET widths. As it is shown, for a small value of W, the open failure probability is the dominant component, and for a large value of W, the short failure probability is the dominant one. The figure indicates that for each CNT synthesis process there is a unique optimum width that leads to the minimum, $P_{\text{F,CNFET}}$. One of the advantages of the proposed statistical model is that the optimum width can be calculated regarding to CNT synthesis parameters. For a particular case, when $P_m = 0.030$ and $\lambda_{s\text{CNT}} = 0.10$, the minimum failure probability is 0.091, which occurs at the optimum point of $W = 24$. Fig. 4 indicates that the total failure probability of a CNFET cannot be improved to a desirable value by using only the sizing technique.

Fig. 5 shows how $P_{\text{F,CNFET}}$ varies with different values of CNT synthesis parameters, i.e., $\lambda_{s\text{CNT}}$ and P_m. As seen, for a fixed value of CNT density, decreasing P_m decreases the failure probability continuously. In contrast, improving the CNT density with a fixed P_m decreases $P_{\text{F,CNFET}}$ to a minimum point and for larger CNT densities, $P_{\text{F,CNFET}}$ increases. The reason of this behavior is that two components of $P_{\text{F,CNFET}}$ ($P_{\text{O,CNFET}}$ and $P_{\text{S,CNFET}}$) exhibit opposite behaviors with respect to a change in CNT density, i.e., increase the CNT density value will increase the $P_{\text{O,CNFET}}$ while it will decrease the $P_{\text{S,CNFET}}$. For small values of $\lambda_{s\text{CNT}}$, $P_{\text{O,CNFET}}$ is dominant in resulting in decreasing $P_{\text{C,CNFET}}$ whereas for larger values of $\lambda_{S\text{CNT}}$, $P_{\text{O,CNFET}}$ is dominant resulting in increasing $P_{\text{F,CNFET}}$.

Considering Fig. 5, it is important to note that for ideal future CNT synthesis process, for example with synthesis parameters $\lambda_{s\text{CNT}} = 0.2$ and $P_m = 0.001$, the total failure probability of a CNFET is in order of 10^{-2}. Therefore, for VLSI integrated circuits with billions of transistors, CNFET failure can substantially reduce the overall circuit yield. Consequently, to achieve practical CNFET-based VLSI circuits with an acceptable functional yield, it is imperative to introduce design techniques to improve the defect tolerance of CNFETs.

IV. Transistor Level Redundancy and CNFET Correlation

Recent approaches of defect tolerance for nano-electronics have focused on adding redundancy at the gate or module level. It has been shown that adding redundancy at the transistor level can provide higher defect tolerance than module and gate levels [26]. In the following, we investigate adding redundancy at the transistor level in the CNT-based technology to reduce the failure probability of CNFETs. We first introduce various structures of transistor level redundancy in CNFET technology, and then, analyze the impacts of CNT correlation on failure probability of each structure.

A. Conventional Transistor Level Redundancy

Fundamentally, the transistor-level redundancy is based on series and parallel connection of devices as shown in Fig. 6(a) and (b). The series transistor structure fails as an open defect if any of the transistors has an open defect. Therefore, the open failure probability in series transistors structure ($P_{\text{O,mSeries}}$) can be derived as follows:

$$P_{\text{O,mSeries}} = 1 - (1 - P_{\text{O,CNFET}})^m \quad (5)$$

where m is the number of transistors used in this structure.

Similarly, a short defect in series structure happens when all transistors functionally fail as a short defect. The short failure probability in this structure ($P_{\text{S,mSeries}}$) can be expressed by

$$P_{\text{S,mSeries}} = {P_{\text{S,CNFET}}}^m. \quad (6)$$

Based on (1), (5), and (6), we can express the total failure probability of series transistor redundancy structure ($P_{\text{F,mSeries}}$) as follows:

$$P_{\text{F,mSeries}} = \left(1 - \left(1 - P_{\text{O,CNFET}}\right)^m\right) + {P_{\text{S,CNFET}}}^m. \quad (7)$$

Using a similar analysis, the total failure probability of parallel transistor redundancy ($P_{\text{F,nParallel}}$) can be derived as

$$P_{\text{O,nParallel}} = {P_{\text{O,CNFET}}}^n \quad (8)$$

$$P_{\text{S,nParallel}} = 1 - (1 - P_{\text{S,CNFET}})^n \quad (9)$$

$$P_{\text{F,nParallel}} = {P_{\text{O,CNFET}}}^n + \left(1 - (1 - P_{\text{S,CNFET}})^n\right) \quad (10)$$

where $P_{\text{O,nParallel}}$ and $P_{\text{S,nParallel}}$ are the open and short failure probabilities in this structure, respectively, and is the number of transistors used in this structure.

Using the proposed model, we compare the failure probability of series and parallel structures in Fig. 7. The value of $P_{\text{O,CNFET}}$ and $P_{\text{S,CNFET}}$ are assumed to be 0.1 and 0.05, respectively. Fig. 7(a) shows the failure probabilities of series and parallel structures (P_F) and their components (P_S and P_O). As it shows, the open failure probability of series (parallel) structures continuously increases (decreases) when the number of redundant transistors increases. On the other hand, the short failure probability of series (parallel) transistors structure decreases (increases) with adding more redundant transistors. As the figure shows, using series and parallel transistors structures does not decrease the total failure probability to an acceptable point. Although, in this case, the total failure probability of series transistors structure decreases

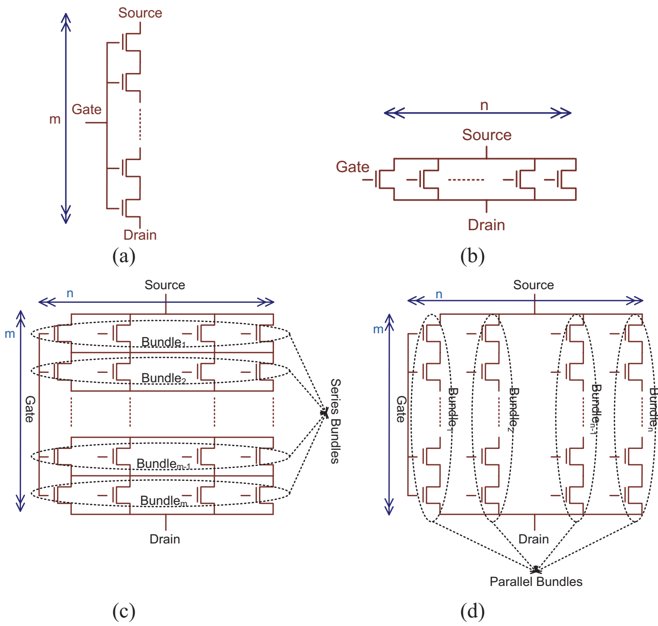


Fig. 6. Different transistor level redundancy structures: (a) series, (b) parallel, (c) series of parallel (SP), and (d) parallel of series (PS).

to a minimum point, but for structures with more redundant transistors, the total failure probability increases. It is notable that this behavior is dependent on the values of $P_{\mathrm{O,CNFET}}$ and $P_{\mathrm{S,CNFET}}$. Fig. 7(b) shows the total failure probabilities of series and parallel structures versus the number of transistors for different values of $P_{\mathrm{O,CNFET}}$ and $P_{\mathrm{S,CNFET}}$. As the figure shows, the minimum achievable total failure probability for these structures is still in the order of 10^{-3}, which is not acceptable for CNFET-based VLSI circuits today.

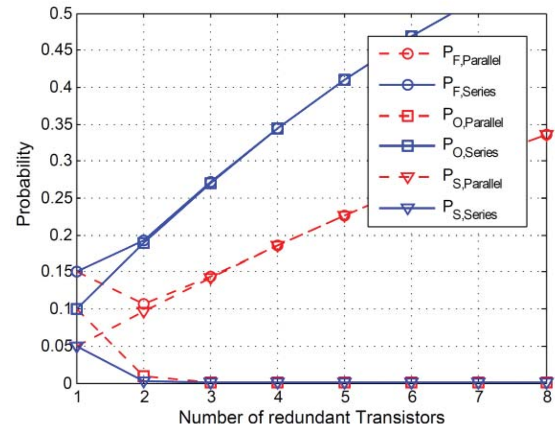
In general, it seems that combining series and parallel transistors structures provides defect tolerance of both open and short defects [24], [25]. Fig. 6(c) and (d) shows the series combination of parallel (SP) and parallel combination of series (PS) structures. In the PS structure, n bundles are connected in a parallel manner where each bundle is construction of m series transistors. In a similar manner, in the SP structure, m bundles are serially connected where each bundle is construction of n parallel transistors.

The SP structure fails as an open circuit if any of the series bundles has an open failure, which means that all parallel transistors in the bundle encounter an open defect. Similarly, a short defect in SP structure occurs when all series bundles fail as a short circuit, which means that any of the parallel transistors in the bundle encounters a short defect. Therefore, the failure probability of the structure ($P_{\mathrm{F,SP}}$) can be expressed as follows:

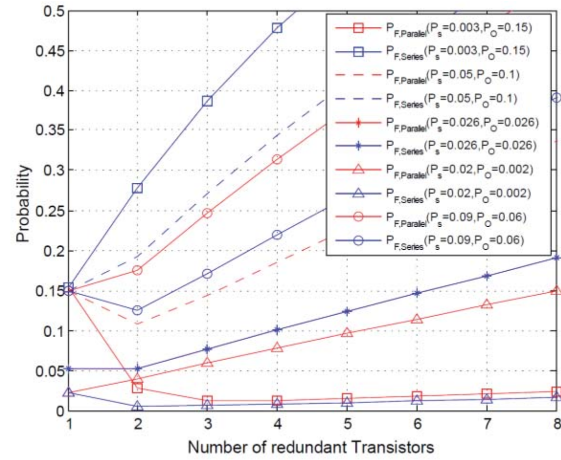
$$P_{\mathrm{O,SP}} = 1 - \left(1 - \left(P_{\mathrm{O,CNFET}}{}^{n}\right)\right)^{m} \tag{11}$$

$$P_{\mathrm{S,SP}} = \left(1 - \left(1 - P_{\mathrm{S,CNFET}}\right)^{n}\right)^{m} \tag{12}$$

$$P_{\mathrm{F,SP}} = 1 - \left(1 - \left(P_{\mathrm{O,CNFET}}{}^{n}\right)\right)^{m} + \left(1 - \left(1 - P_{\mathrm{S,CNFET}}\right)^{n}\right)^{m} \tag{13}$$



(a)



(b)

Fig. 7. (a) Total failure probability of series and parallel structures and its components versus the number of transistors. (b) Total failure probability of series and parallel structures for various P_o and P_s.

where n is the number of parallel transistors in each bundle and m is the number of series bundles.

In the same way, the failure probability of the PS structure ($P_{\mathrm{F,PS}}$) is as follows:

$$P_{\mathrm{O,PS}} = \left(1 - \left(1 - P_{\mathrm{O,CNFET}}\right)^{m}\right)^{n} \tag{14}$$

$$P_{\mathrm{S,PS}} = 1 - \left(1 - P_{\mathrm{S,CNFET}}{}^{m}\right)^{n} \tag{15}$$

$$P_{\mathrm{F,PS}} = \left(1 - \left(1 - P_{\mathrm{O,CNFET}}\right)^{m}\right)^{n} + 1 - \left(1 - P_{\mathrm{S,CNFET}}{}^{m}\right)^{n} \tag{16}$$

where m is the number of series transistors in each bundle and n is the number of parallel bundles.

Fig. 8 shows the total failure probability of SP and PS structures versus m and n where the values of $P_{\mathrm{O,CNFET}}$ and $P_{\mathrm{S,CNFET}}$ are assumed to be 0.1 and 0.05, respectively. Fig. 8 demonstrates that the total failure probability of both structures can be reduced to a desired point with choosing suitable m and n values. For example, in this case, the total failure probability of 7.1×10^{-4} (6.1×10^{-4}) can be achieved for $m = 5(4)$ and $n = 4(7)$ in the SP (PS) structure. Consequently, SP and PS structures can be applied for enhancing the defect tolerance of

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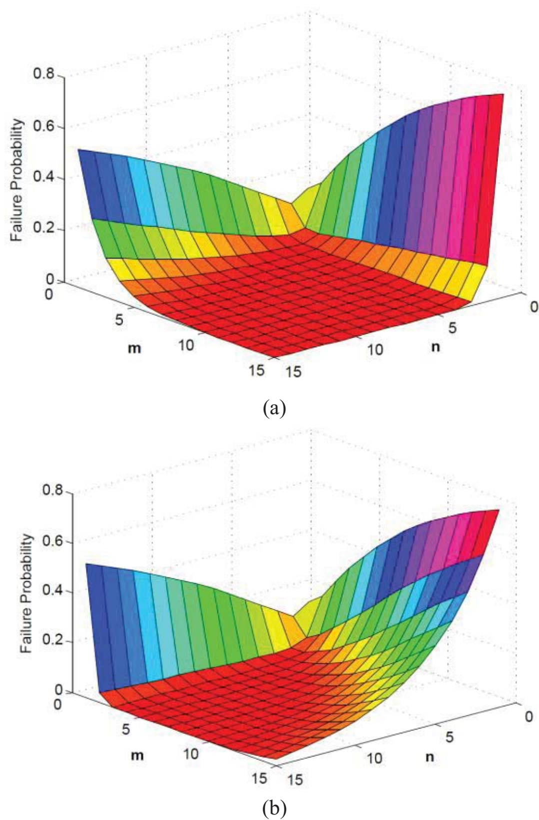
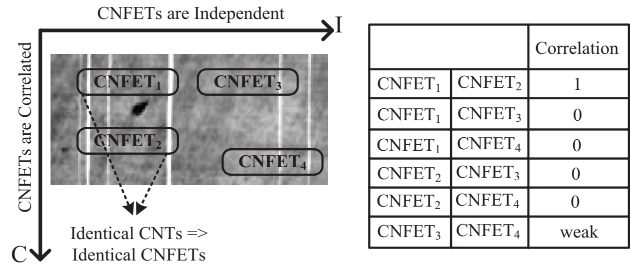


Fig. 8. Total failure probability versus m and n. (a) SP. (b) PS structures.

circuits for conditions in which both open and short defects are probable.

B. CNFETs Correlation Effects

It is more important to note that the analysis provided in the previous section is based on the assumption that the open (and short) defects of all transistors are fully independent. However, CNFETs fabricated on aligned CNTs have an inherent correlation [13]. Furthermore, the correlation is an isotropic, i.e., the correlation is nonuniform in all orientations. On the other hand and more importantly, an additional characteristic of CNFETs placed on aligned CNTs is that CNFETs along one orientation are completely independent of one another. For the purpose of illustration, consider four CNFETs fabricated adjacent to each other shown in Fig. 9. CNFET_1 and CNFET_2 consist of the same CNTs (different segments of the same CNTs). Thus, we can conclude that, if CNFET_1 contains one m-CNT and two s-CNTs, then CNFET_2 also contains exactly one m-CNT and two s-CNTs. So, CNFETs aligned along the CNT growth direction are highly correlated. Next, consider CNFET_1 and CNFET_3 fabricated horizontally side by side (Fig. 9). These two CNFETs consist of different CNTs in their active regions. Due to the fact that CNTs are grown and aligned independently [8], they have no common CNT, and thus, we cannot say much about CNFET_3, even if we know that CNFET_1 has any m- or s-CNTs. That is, CNFETs which are not aligned and do not have any overlapping section along the CNT growth direction and are completely independent. Note that CNFETs which are not



		Correlation
CNFET_1	CNFET_2	1
CNFET_1	CNFET_3	0
CNFET_1	CNFET_4	0
CNFET_2	CNFET_3	0
CNFET_2	CNFET_4	0
CNFET_3	CNFET_4	weak

Fig. 9. Illustration of single-directional correlation and single-directional independence that are inherent in CNFETs fabricated on aligned CNTs. Table shows the correlation values for CNFETs shown in the figure (1 = fully correlated and 0 = fully uncorrelated) [17].

aligned along the CNT growth direction but have overlapping sections along the CNT growth direction (consider CNFET_3 and CNFET_4 in Fig. 9) have a weak correlation.

For ease of analysis, we make the following simplifying assumptions regarding to single-directional correlation and independence (In the rest of this paper, we refer to these assumptions as *CI assumptions*) [17].

1) CNFETs along the I-direction are independent (thus, the I-direction correlation is zero). I-direction refers to the direction perpendicular to the CNT growth direction (Fig. 9).
2) CNFETs along the C-direction are identical (thus, the C-direction correlation is one). C-direction refers to the CNT growth direction (Fig. 9).

Because of the single-directional correlation in CNFET technology, the failure probability of series and parallel transistors is affected by the layout placement of redundant transistors. In this paper, we only focus on two cases: all CNFETs are aligned along either C-direction or I-direction.

By connecting m transistors in series along the C-direction, the Correlated-mSeries structure (*C-mSeries*) is obtained [Fig. 10(a)]. It is important to note that the failure probability of this structure remains unchanged compared to a single CNFET because all CNFETs are identical (perfectly correlated) under the CI assumption. That is, there are only two possibilities: either all CNFETs are functional, or all CNFETs are defective, and thus, the failure probability of C-mSeries is the same as the failure probability of a single CNFET. Hence, the total failure probability of C-mSeries structure ($P_{\text{F,C,mSeries}}$) can be written as follows:

$$P_{\text{F,C}-\text{mSeries}} = P_{\text{F,CNFET}}. \tag{17}$$

Using a similar definition, we call the redundancy structure with m series transistors aligned along I-direction as the Independent m-Series (*I-mSeries*) structure [Fig. 10(b)]. Since all transistors in this structure are independent, the total failure probability of I-nSeries ($P_{\text{F,I}-\text{nSeries}}$) can be derived as follows:

$$P_{\text{F,I}-\text{mSeries}} = P_{\text{F,m}-\text{Series}} \tag{18}$$

where $P_{\text{F,m}-\text{Series}}$ is derived from (7).

Parallel CNFET structures can be fabricated aligned along C- or I-direction on CNTs. Using an analysis similar to series CNFET cases, the total failure probability of Correlated-nParallel (*C-nParallel*) and Independent-nParallel (*I-nParallel*)

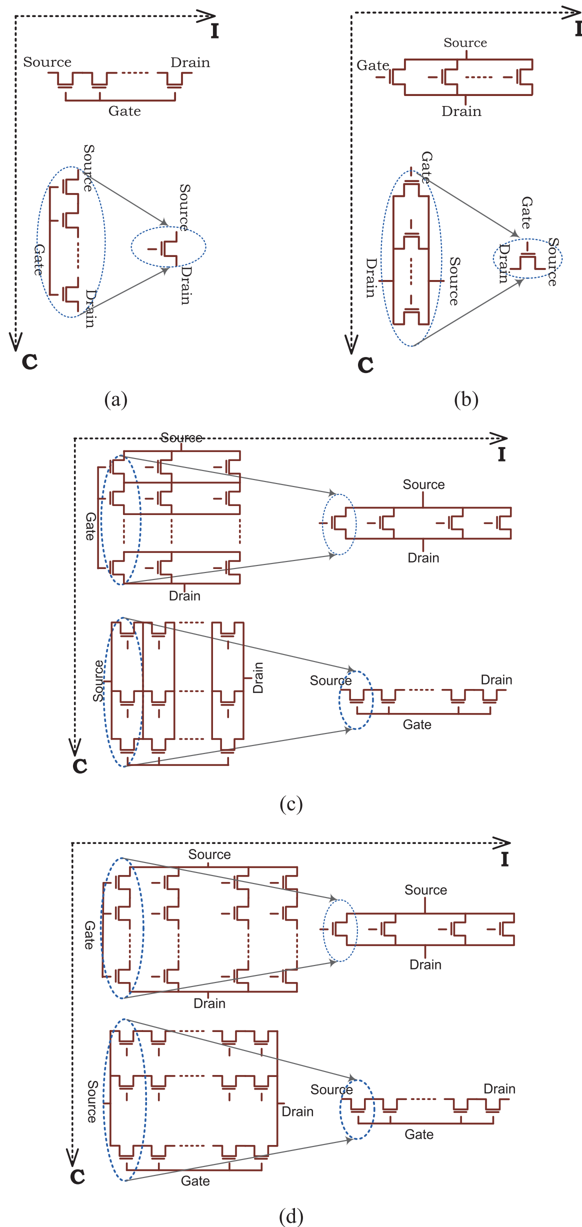


Fig. 10. Different implementations of various redundant structures considering CNFETs correlation. The circuit on the left shows the implementations and the one on the right represent the circuit with equivalent failure probability. (a) Series structures. (b) Parallel structures. (c) PS structure. (d) SP structure.

structures are calculated as

$$P_{\mathrm{F,C-nParallel}} = P_{\mathrm{F,CNFET}} \tag{19}$$

$$P_{\mathrm{F,I-nParallel}} = P_{\mathrm{F,nParallel}} \tag{20}$$

where $P_{\mathrm{F,C-nParallel}}$ and $P_{\mathrm{F,I-nParallel}}$ are the total failure probability of C-nParallel and I-nParallel structures, respectively, and $P_{\mathrm{F,nParallel}}$ is derived from (10).

CNFET correlation can affect defect tolerance characteristics of SP and PS structures as well. We consider two implementations of the PS structures in CNFET technology as depicted in Fig. 10(c). I-nParallel/C-mSeries (InP/CmS) and C-nParallel/I-mSeries (CnP/ImS) structures. In InP/CmS, the m series transistors in each bundle are aligned in the CNT growth direction. So, these transistors are fully correlated, and thus, identical. On the other hand, the n parallel bundles are independent. Consequently, the total failure probability of InP/CmS structure is equal to the total failure probability of I-nParallel one. In contrast, in CnP/ImS, the n bundles are aligned in the CNT growth direction, and so, are identical. On the other hand, the m series transistors in each bundle are independent. So, the total failure probability of CnP/ImS implementation is equal to the total failure probability of I-mSeries structure. Overall, we have

$$P_{\mathrm{F,InP/CmS}} = P_{\mathrm{F,I-nParallel}} \tag{21}$$

$$P_{\mathrm{F,CnP/ImS}} = P_{\mathrm{F,I-mSeries}} \tag{22}$$

where $P_{\mathrm{F,InP/CmS}}$ and $P_{\mathrm{F,CnP/ImS}}$ are the total failure probability of InP/CmS and CnP/ImS structures, respectively.

Similarly, SP structures can be implemented in two ways: I-mSeries/C-nParallel (ImS/CnP) and C-mSeries/I-nParallel (CmS/InP) [Fig. 10(d)]. Transistors in each bundle in ImS/CnP implementation are identical and the failure probability of this implementation is the same as the failure probability of I-mSeries. Using a similar analysis, the failure probability of CmS/InP equals the failure probability of I-nParallel structure as the bundles are fully correlated. Therefore, we have

$$P_{\mathrm{F,ImS/CnP}} = P_{\mathrm{F,I-mSeries}} \tag{23}$$

$$P_{\mathrm{F,CmS/InP}} = P_{\mathrm{F,I-nParallel}} \tag{24}$$

where $P_{\mathrm{F,ImS/CnP}}$ and $P_{\mathrm{F,CmS/InP}}$ are the total failure probability of ImS/CnP and CmS/InP structures, respectively.

Fig. 10 shows Independent and Correlated aligned implementation of different redundant transistor structures and the corresponding circuits with equal total failure probability. As can be seen, both SP and PS implementations in CNFET technology have a total failure probability equal to either series or parallel structures. Based on the results shown in Section IV-A, these types of redundancy cannot be applied for enhancing the yield of CNFET circuits in which both open and short defects are probable. Consequently, in order to take advantage of transistor redundancy techniques, it is necessary to present efficient solutions considering CNFET correlation characteristics.

V. Proposed CNFET Redundant Structure

Based on the analysis provided in the previous section, the failure probability of CNFETs in SP and PS structures can be lowered by eliminating or reducing correlation of such structures.

Using this idea, we propose *independent Series/Parallel* (*ISP*) and *independent Parallel/Series* (*IPS*) structures to reuse the advantages of SP and PS defect-tolerant techniques in CNFET technology. In the proposed structures, transistors are placed such that there is no overlapping section between the bundles and the transistors in each bundle. The proposed structures are shown in Fig. 11. It is important to note that the total failure probabilities of ISP and IPS structures are equal to those of SP and PS structures, respectively. That is

$$P_{\mathrm{F,ISP}} = P_{\mathrm{F,SP}} \tag{25}$$

$$P_{\mathrm{F,IPS}} = P_{\mathrm{F,PS}} \tag{26}$$

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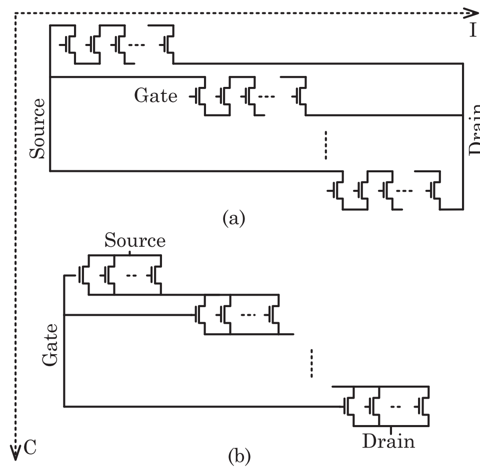

Fig. 11. Proposed independent (a) SP and (b) PS structures. The transistors are placed such that there is no overlapping section between the bundles and the transistors in each bundle.

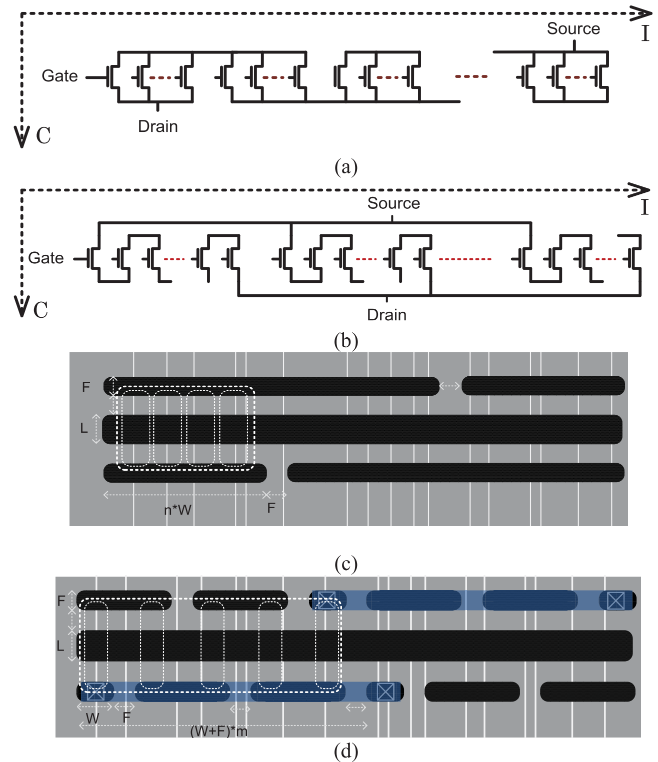

Fig. 12. (a) Proposed ISP implementation. (b) Proposed IPS implementation. (c) Layout of ISP implementation on aligned CNTs (similar to [17]). (d) Layout of IPS implementation on aligned CNTs. Metal layer 2 is used to connect the source (drain) of corresponding transistors.

where $P_{\mathrm{F,ISP}}$ and $P_{\mathrm{F,IPS}}$ are the total failure probabilities of ISP and IPS, respectively.

Implementations of ISP and IPS, as shown in Fig. 11, need extra connections and result in unused area, leading to large area overhead. To reduce the area overhead, bundles in the ISP and IPS structures are placed in the form shown in Fig. 12(a) and (b), respectively. Fig. 12(c) and (d) shows the proposed layout diagram for a sample ISP and IPS structures. In ISP layout, the parallel transistors are implemented using a single transistor which has a width equal to the sum of the width of parallel transistors. These wide transistors are connected in series and aligned in I-direction. In IPS layout, the series transistors are aligned in I-direction. To connect the source (and drain) of transistors in each bundle to the source (and drain) of corresponding transistors in the other bundle, we use metal layer 2 as shown in Fig. 12(d).

Although ISP and IPS structures can be used as defect tolerant techniques in CNFET technology, as (13) and (16) show, different values of P_O and P_S affect the total failure probability of each technique in a different way. To reveal the difference, we analyze the impacts of P_O and P_S on the total failure probability of ISP and IPS structures. Fig. 13(a)–(c) show the subtraction values of IPS failure probability ($P_{\mathrm{F,IPS}}$) and ISP failure probability ($P_{\mathrm{F,ISP}}$), i.e., $P_{\mathrm{F,IPS}} - P_{\mathrm{F,IPS}}$ for three different situations: $m<n$, $m = n$, and $m>n$. As Fig. 13 shows, for different cases, finding a specific $m \times n$ structure with lower total failure probability is completely dependent on the values of P_O and P_S. For example, consider the situation $m = n = 3$ in Fig. 13(a). For cases in which the value of $P_O(P_S)$ is less than $P_S(P_O)$, the total failure probability of ISP (IPS) structure is dominant. This means that if fabrication technology provides larger P_S comparing to P_O, for example when no m-CNT removal is applied, reduction of the total failure probability is recommended to the ISP structure. On the other hand, if fabrication technology decreases P_S by using m-CNT removal techniques, the IPS structure is more suitable to be used to fabricate defect tolerant circuits. In addition, Fig. 13(a) (Fig. 13(c)) shows that ISP (IPS) is more efficient in different fabrication technology conditions in the case $m<n(m>n)$.

As (13) and (16) show, IPS and ISP structures trade area, i.e., the number of transistors, to achieve both m-CNT and nonuniform CNT tolerance. Thus, there is a tradeoff that needs to be considered in order to design optimal defect tolerant CNFET-based circuits under various design goals.

In most cases, it is important that the failure probability becomes less than a specific threshold value, a requirement that we call *Failure Probability Threshold* (*FPT*) constraint, with a minimum design overhead such as area. In fact, m and n parameters can be optimized such that, based on a specific P_O and P_S, the FPT constraint is satisfied. On the other hand, as mentioned before in Section IV-A and based on (25) and (26), ISP (SP) and IPS (PS) structures have different total failure probability values for the same (m,n) parameters (see Section IV-B). Consequently, for a typical fabrication process with a specific P_O and P_S, it is advantageous to know which ISP or IPS structures (and also which values of m and n) satisfy the FPT constraint with less area overhead. In the following, we present a method to find the efficient redundancy structure which satisfies FPT constraint with the least design overhead.

We call the set of ordered pairs containing possible values for (m,n) the set of *feasible pairs* if the total failure probability of the corresponding ISP (or IPS) is less than the FPT value. For different cases with different design parameters, feasible pairs can be revealed using (13) and (16). Considering the

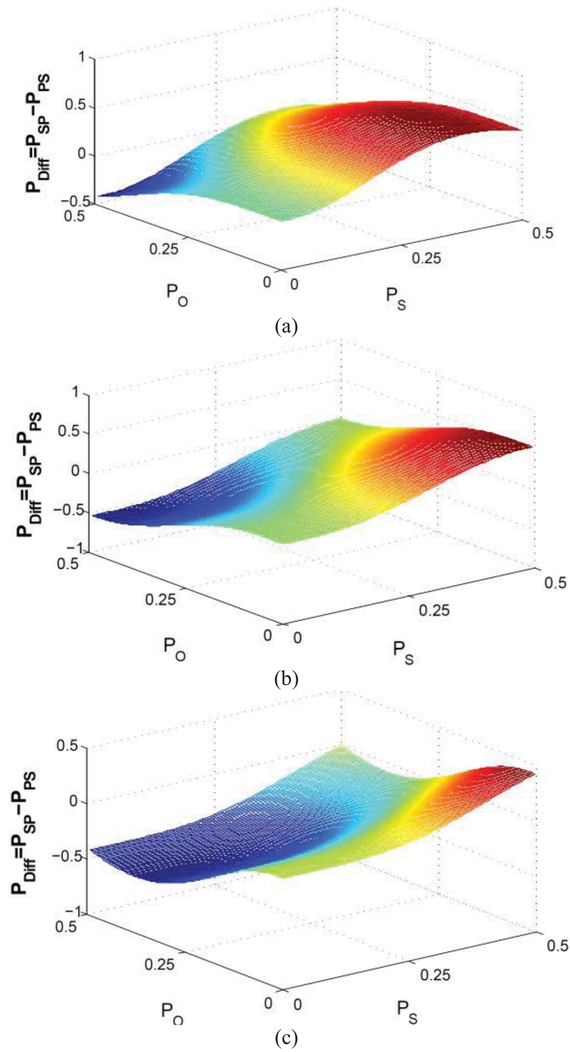

Fig. 13. Comparing failure probability of ISP and IPS structure for different values of P_o and P_s (a) $m = n = 3$, (b) $m < n$, and (c) $m > n$.

area overhead, we have to choose a pair (m,n) such that the number of transistors, i.e., $m \times n$, is minimized. We call this ordered pair the *optimal pair*.

In order to find the optimal pair, it is necessary to consider the feasible pairs of both ISP and IPS structures simultaneously. We consider the union of the feasible pairs of both ISP and IPS in a new set called *joint feasible pairs*. To obtain the most area-efficient defect-tolerant structure, the optimal pair of the joint feasible pairs provides the value of (m,n) pair and the location of optimal pair determines the type of the structure, ISP or IPS (ISP in this example). It is notable that the optimal pair can be in the intersection region of ISP and IPS feasible pairs. In this case, either ISP or IPS can be chosen based on the other design parameters.

For example, Fig. 14 shows the joint feasible pairs for the case shown in Fig. 8 with FPT $= 0.005$. In fact, the total failure probability of all structures with (m, n) shown in Fig. 14 is less than 0.005. Among these possible solutions, choosing $m = 2$ and $n = 4$ leads to the minimum area overhead. So (2, 4) is the optimal point.

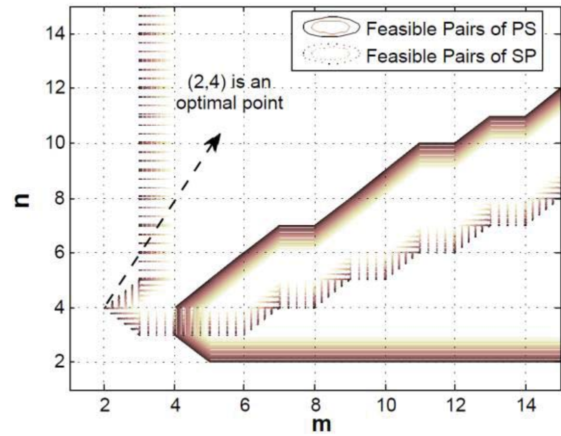

Fig. 14. Feasible pairs for ISP and IPS and joint feasible pairs.

VI. Design Space Analysis and Tradeoffs

This section analyzes the tradeoffs that need to be considered in order to take advantage of the proposed techniques. Furthermore, these analyses will set forth target guidelines for material development, such as the required CNT density variation and percentage of s-CNTs, so as to achieve practical CNFET-based VLSI circuits.

Applying redundant transistors to reduce the circuit failure probability (P_F) impacts design metrics including the circuit area (A) as well as the transistors current drive (I_{drive}). The design metrics depend on the CNT chemical synthesis parameters, i.e., λ_{CNT} and P_m, in addition to CNFET structure parameters, i.e., W, m, and n. Thus, the following analyses look at how the proposed method impacts the design metrics (P_F, I_{drive}, A), given the CNT process synthesis parameters (λ_{CNT}, P_m).

We assume that each CNFET in the SP (or PS) structure carries the same current when the gate is ON and denotes this as I_{CNFET}. In addition, we assume that the currents of IPS (I_{ISP}) and ISP (I_{ISP}) proportionally decrease with the number of CNFETs in series (i.e., m) and increase with the number of CNFETs in parallel, n. Thus

$$I_{\text{IPS}} = I_{\text{ISP}} \approx \frac{n}{m} \times I_{\text{CNFET}} \approx \frac{n}{m} \times \frac{W}{L}. \tag{27}$$

However, the above equation is true for the defect-free case. The current of a redundant structure is proportional to the effective width (W_e) and effective length (L_e) of the structure which are affected by the short and open defects. Using a probabilistic approach, the current drive can be calculated by

$$I_{\text{IPS(ISP)}} = \sum_{i \in DS} P_{S,i} I_{S,i} \tag{28}$$

where $P_{S,i}$ shows the probability that the ISP(IPS) is transformed to configuration i in the presence of defects, is the current of configuration i and is the set of all possible configurations created from IPS (ISP) structure under the defects.

For the sake of simplicity, we approximate the currents under defects by

$$I_{\text{IPS}} = I_{\text{ISP}} \approx \frac{W_e}{L_e} \times I_{\text{CNFET}} \approx \frac{(1 - P_{O,\text{CNFET}})n}{(1 - P_{S,\text{CNFET}})m} \times \frac{W}{L}. \tag{29}$$

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TABLE I

TRADEOFFS OF CNFET, IPS, AND ISP FOR VARIOUS CNT SYNTHESIS AND DESIGN PARAMETERS

CNT synthesis and design parameters				Optimized for area								Optimized for current drive							
				IPS				*ISP*				*IPS*				*ISP*			
λ_{CNT}	P_m	Y	Y_{chip}	m	n	I_{drive}/I_{CNFET}	A_{AIPS}/A_{CNFET}	m	n	I_{drive}/I_{CNFET}	A_{AIPS}/A_{CNFET}	m	n	I_{drive}/I_{CNFET}	A_{AIPS}/A_{CNFET}	m	n	I_{drive}/I_{CNFET}	A_{AIPS}/A_{CNFET}
0.15	10^{-3}	32	90%	4	4	1.003	17.00	4	3	0.752	15.00	4	4	1.003	17.00	5	5	1.003	31.25
0.2	10^{-3}	32	90%	4	3	0.754	13.00	5	3	0.603	18.75	4	4	1.006	17.00	5	5	1.006	31.25
0.5	10^{-3}	32	90%	4	1	0.254	5.00	4	1	0.254	5.00	5	5	1.016	26.25	8	8	1.016	80.00
0.2	10^{-4}	32	90%	3	3	1.000	9.75	3	3	1.000	11.25	3	3	1.000	9.75	3	3	1.000	11.25
0.5	10^{-4}	32	90%	3	1	0.333	3.75	3	1	0.333	3.75	3	3	1.001	9.75	4	4	1.001	20.00
0.15	10^{-2}	32	80%	6	4	0.698	25.50	8	3	0.392	30. 00	6	6	1.047	37.5	8	3	0.523	62.50
0.2	10^{-2}	32	80%	7	3	0.458	22.75	8	2	0.267	20	7	7	1.069	50.75	8	2	0.267	20.00
0.1	10^{-3}	32	80%	3	5	1.658	15.75	4	4	0.994	20.00	5	5	0.994	26.25	4	4	0.994	20.00
0.2	10^{-3}	32	80%	4	3	0.754	13.00	4	2	0.503	10.00	4	4	1.006	17.00	5	5	1.006	31.25
0.15	10^{-4}	32	80%	3	3	0.999	9.75	3	3	0.999	11.25	3	3	0.999	9.75	3	3	0.999	11.25
0.5	10^{-4}	32	80%	3	1	0.333	3.75	3	1	0.333	3.75	3	3	1.001	9.75	3	3	1.001	11.25
0.3	10^{-2}	16	70%	6	4	0.698	25.5	8	3	0.392	30.00	6	6	1.047	37.5	13	8	0.644	130.0
0.5	10^{-2}	16	70%	7	2	0.309	15.75	8	2	0.270	20.00	7	7	1.083	50.75	8	2	0.270	20.00
0.3	10^{-3}	16	70%	4	3	0.752	13.00	4	3	0.752	15.00	4	4	1.003	17.00	4	4	1.003	20.00
0.5	10^{-3}	16	70%	4	2	0.504	9.00	4	2	0.504	10.00	4	4	1.008	17.00	5	5	1.008	31.20
0.3	10^{-4}	16	70%	3	3	0.999	9.75	3	3	0.999	11.25	3	3	0.999	9.75	3	3	0.999	11.25
0.5	10^{-4}	16	70%	3	2	0.667	6.75	3	2	0.667	7.50	3	3	1.000	9.75	3	3	1.000	11.25

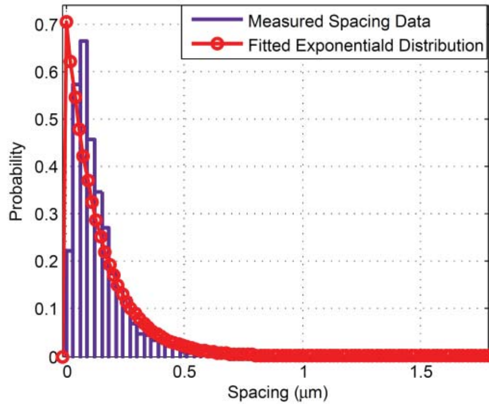

Fig. 15. Probability distribution function (PDF) of CNT spacing.

It is notable that, for defect-free case ($P_{O,\text{CNFET}} = P_{S,\text{CNFET}} = 0$), (29) will be transformed to (27).

To arrive at an analytical expression for area, ISP and IPS layout rules must be defined. Without loss of generality, we approximate the CNFET, ISP, and IPS area as follows:

$$\text{Area}_{\text{CNFET}} = (L + 4F)W \quad (30)$$

$$\text{Area}_{\text{ISP}} = (L + 4F)\Big(\big((n \times W) + F\big) \times m\Big) \quad (31)$$

$$\text{Area}_{\text{IPS}} = (L + 4F)\Big(\big(m \times (W + F)\big) \times n\Big) \quad (32)$$

where F is the lithographic half-pitch (minimum feature size) and L is the CNFET length (see Figs. 1 and 13). Assuming $W = 4F$, (31) and (32) show that ISP has a lower area overhead comparing to IPS structure for a given m and n.

To investigate the tradeoffs between various parameters in CNFET, ISP, and IPS structures, we have to determine the total failure probability, P_F, based on a targeted chip functional yield, Y_{chip}. Consider a chip designed using CNFET technology has N_T transistors. To achieve a predetermined Y_{chip}, the total failure probability of each CNFET must be less than a constraint as follows:

$$\text{Functional Yield} \geq Y_{\text{chip}} \Rightarrow (1 - P_F)^{N_T} \geq Y_{\text{chip}} \Rightarrow P_F \leq 1 - \left(Y_{\text{chip}}\right)^{\frac{1}{N_T}}. \quad (33)$$

TABLE II

COMPARISON OF STATISTICAL–BASED AND MC SIMULATION-BASED $P_{O,\text{CNFET}}$ ESTIMATION

CNFET width (W)	$P_{O,\text{CNFET}}$ using (A.12)	$P_{O,\text{CNFET}}$ using MC simulation	Error[(statistical−MC)/MC]%
0.5 μm	0.6174	0.6307	2.10%
1.0 μm	0.4402	0.4469	1.49%
2.0 μm	0.2478	0.2482	0.16%
5.0 μm	0.0583	0.0585	0.34%

However, considering CNT growth imperfections and P_F variations often does not satisfy the yield constraint in VLSI circuits. For example, for the case $N_T = 10^7$ and $Y_{\text{chip}} = 80\%$, the total failure probability of each CNFET must be at least 2×10^{-7} which is not easy to get considering the current CNT synthesis processes [10], [11]. Hence, ISP or IPS structures can be exploited to satisfy the failure probability constraint.

Table I shows the tradeoffs for different CNT synthesis and design parameters for ISP and IPS structures. In this analysis, N_T is assumed to be 10^7 and for each set of CNT synthesis and design parameters, two pairs of m and n are chosen to

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reduce either area or current drive overheads. It is notable that the functional yield for a single CNFET, i.e., without any redundancy, is approximately equal to zero for all synthesis parameters shown in Table I.

According to the results shown in Table I, for a single CNFET, the acceptable functional yield cannot be achieved even with upcoming CNT synthesis with ideal parameters (e.g., $\lambda_{\mathrm{CNT}} = 0.5$, $P_m = 10^{-4}$). So, using redundant transistor structure is an unavoidable solution to achieve an acceptable functional yield in CNFET technology. On the other hand, using redundant transistor structures without synthesis parameter enhancement imposes considerable design overheads. As a result, to take advantage of CNFET technology, it is necessary to use efficient redundant structures such as the proposed method in addition to improving the CNT synthesis processes. In other words, joint co-optimization of design and processing is necessary for imperfection-immune CNFET circuits considering metallic CNTs and CNT density variations.

VII. Conclusion

Using experimental data from aligned CNTs, a new statistical failure probability model for CNFETs has been presented. The new compact failure model takes into account major CNFET nonidealities including metallic CNTs and CNT density variation. The proposed model is used to indicate the limitations of current CNT synthesis processes in designing CNFET-based VLSI circuits with acceptable functional yield. A detailed analytical study on various structures of transistor redundancy concept in CNFET technology has been presented in terms of failure probabilities. Then, we proposed ISP and IPS structures based on combinations of series and parallel transistors considering CNT correlation in order to enhance the functional yield of CNFET circuits. Experimental results have demonstrated that the proposed technique can reach a targeted functional yield for different CNT process synthesis parameters in expense of area and/or current drive overheads.

The proposed defect tolerant technique can be extended to be applied in the chip level to help reduce the area overhead, i.e., use correlated CNFETs to build circuits. In addition, ISP/IPS is a design concept that can be applicable in other fields, such as nanowire transistors or other 1-D devices. In this paper, we have applied the proposed statistical failure model in a few applications, whereas the model can be explored to many other applications such as CNFET device modeling.

In conclusion, ISP/IPS marks the first demonstration of a VLSI-compatible CNFET design methodology and represents a new approach toward solving the metallic and nonuniform CNTs problem. By overcoming one of the major barriers toward CNFET-based circuits, ISP/IPS allows CNT technology to propel forward as a potential candidate for VLSI beyond silicon CMOS.

Appendix A

Derivation of CNFET Failure Probability

We use the CNT spacing data, i.e., the distance between neighboring CNTs and is denoted by S_{CNT}, to estimate the open and short failure probability of a CNFET. CNT spacing statistical distribution is extracted from atomic force microscopy (AFM) images of aligned CNTs grown on quartz wafers. Aligned CNTs were grown on quartz substrate using guided chemical vapor deposition (CVD) process [10]. We perform image processing on such AFM images to extract the statistical distribution of CNT spacing. Fig. 12 shows the CNT spacing distribution extracted from AFM images of CNTs by considering all possible pairs of adjacent CNTs in the images. Based on the obtained results, a parameterized analytical model is fitted to the experimentally extracted CNT spacing distribution. The statistical distribution of CNT spacing, $\mathbb{S}_{\mathrm{CNT}}$, can be approximated by using an exponential random variable with distribution parameter $\lambda_{S_{\mathrm{CNT}}}$

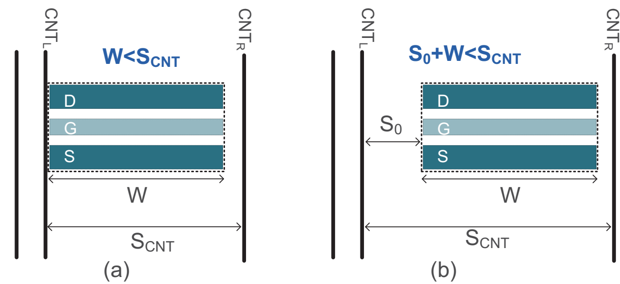

Fig. 16. Void CNFET. (a) CNT_L is placed on the left side of CNFET. (b) There is a distance, S_0, between CNT_L and the left side of CNFET.

$$\mathbb{S}_{\mathrm{CNT}} \sim \mathrm{Exponential}\big(\lambda_{S_{\mathrm{CNT}}}\big) \tag{A.1}$$

$$P(\mathbb{S}_{\mathrm{CNT}} = S_{\mathrm{CNT}}) = \lambda_{S_{\mathrm{CNT}}} e^{-\lambda_{S_{\mathrm{CNT}}} S_{\mathrm{CNT}}}. \tag{A.2}$$

Using the well-known maximum likelihood approach [19] to estimate the distribution parameter, $\lambda_{S_{\mathrm{CNT}}}$ can be calculated with negligible errors.

Fig. 15(b) compares the CNT spacing distribution extracted from AFM images of CNTs with the proposed exponentially modeled CNT spacing distribution. As can be shown, the predicted model produces similar results to the experimentally extracted distribution. It is notable that the measured data and the analytical model do not exactly match. However, this difference leads to a negligible error in the failure probability prediction (see the results of the corresponding studies in Table II.) Moreover, this modeling error will be decreased in future CNT synthesis processes [11] as increasing the tube density intuitively causes the mean value of the measured spacing data values to be decreased.

To derive the open failure probability, we follow two examples of void CNFETs shown in Fig. 16(a) and (b). In these situations, a CNFET is placed between two CNTs, i.e., CNT_L and CNT_R. First, we consider the case in which the left side of the CNFET is placed to the right of the CNT_L by an infinitesimal amount [Fig. 16(a)]. In that case, if the CNFET width (W) is less than $\mathbb{S}_{\mathrm{CNT}}$, there will be no CNT in the active region leading to an open defect. As a result, the open failure probability is equal to the probability that $\mathbb{S}_{\mathrm{CNT}}$ is larger than W

$$P_{O,\mathrm{CNFET}} = P(W \leq \mathbb{S}_{\mathrm{CNT}}). \tag{A.3}$$

Equation (A.3) calculates $P_{O,\mathrm{CNFET}}$ for the cases in which the left side of the CNFET is to the right of CNT_L. However, in

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reality, the left side of the CNFET can be placed at any random position with equal probability for all positions between CNT_L and CNT_R. As a result, the distribution of the spacing between the left side of the CNFET and the CNT_L, denoted by $\mathbb{S}_0$, can be approximated by a continuous uniform distribution with parameters 0 and S_{CNT}. So, for a fixed S_{CNT}, the probability distribution of $\mathbb{S}_0$ is as follows:

$$P(\mathbb{S}_0 = S_0) = \begin{cases} \frac{1}{S_{\text{CNT}}}, & 0 < S_0 < S_{\text{CNT}} \\ 0, & 0 \geq S_0, S_0 \leq S_{\text{CNT}}. \end{cases} \quad \text{(A.4)}$$

In this case, if the value of $\mathbb{S}_0 + W$ is less than $\mathbb{S}_{\text{CNT}}$, there will be no CNT in the active region of CNFET leading to an open defect. As a result, the open failure probability can be expressed as

$$P_{O,\text{CNFET}} = P(\mathbb{S}_0 + W \leq \mathbb{S}_{\text{CNT}}). \quad \text{(A.5)}$$

To derive a compact model for $P_{O,\text{CNFET}}$, using the total probability theorem [19], (A.5) can be rewritten as follows:

$$P(\mathbb{S}_0 + W \leq \mathbb{S}_{\text{CNT}}) = \int_0^{+\infty} P(\mathbb{S}_{\text{CNT}} = S_{\text{CNT}}) P(\mathbb{S}_0 + W \leq S_{\text{CNT}} \mid \mathbb{S}_{\text{CNT}} = S_{\text{CNT}}) ds_{\text{CNT}} \quad \text{(A.6)}$$

where $P(\mathbb{S} + W \leq S_{\text{CNT}} | S_{\text{CNT}} = S_{\text{CNT}})$ is the conditional probability of $\mathbb{S}_0 + W \leq S_{\text{CNT}} = S_{\text{CNT}}$ given $\mathbb{S}_{\text{CNT}} = S_{\text{CNT}}$.

To derive the conditional term of (A.6), we first use the conditional form of (A.4) and then, derive the corresponding cumulative distribution function. Hence

$$P(\mathbb{S}_0 = S_0 \mid \mathbb{S}_{\text{CNT}} = S_{\text{CNT}}) = \begin{cases} \frac{1}{S_{\text{CNT}}}, & 0 < S_0 < S_{\text{CNT}} \\ 0, & 0 \geq S_0, S_0 \leq S_{\text{CNT}} \end{cases} \quad \text{(A.7)}$$

$$P(\mathbb{S}_0 \leq S_0 \mid \mathbb{S}_{\text{CNT}} = S_{\text{CNT}}) = \begin{cases} 0, & S_0 \leq 0 \\ \int_0^{S_0} \left(\frac{1}{S_{\text{CNT}}} du \right) = \frac{S_0}{S_{\text{CNT}}}, & 0 < S_0 < S_{\text{CNT}} \\ 1, & S_{\text{CNT}} \leq S_0. \end{cases} \quad \text{(A.8)}$$

Considering (A.8), we can express the conditional term of (A.6) as

$$P(\mathbb{S}_0 \leq S_{\text{CNT}} - W \mid \mathbb{S}_{\text{CNT}} = S_{\text{CNT}}) = \begin{cases} 0, & S_{\text{CNT}} \leq W \\ \frac{S_{\text{CNT}} - W}{S_{\text{CNT}}}, & 0 < W \leq S_{\text{CNT}}. \end{cases} \quad \text{(A.9)}$$

Therefore, considering (A.2) and (A.9), the integral in (A.6) can be calculated as follows:

$$\begin{aligned} P(\mathbb{S}_0 + W \leq \mathbb{S}_{\text{CNT}}) &= \int_0^{+\infty} \left(\begin{cases} 0 & S_{\text{CNT}} \leq W \\ \lambda_{S_{\text{CNT}}} e^{\lambda_{s_{\text{CNT}}} s_{\text{CNT}}} \left(\frac{S_{\text{CNT}} - W}{S_{\text{CNT}}} \right) & W \leq S_{\text{CNT}} \end{cases} \right) dS_{\text{CN}} \\ &= e^{-\lambda_{s_{\text{CNT}}} W} - W \lambda_{S_{\text{CNT}}} \int_W^{+\infty} - \frac{e^{\lambda_{s_{\text{CNT}}} s_{\text{CNT}}}}{S_{\text{CNT}}} dS_{\text{CNT}}. \end{aligned} \quad \text{(A.10)}$$

Using a change of variables technique, we have

$$P(\mathbb{S}_0 + W \leq \mathbb{S}_{\text{CNT}}) = e^{-\lambda_{S_{\text{CNT}}} W} - W \lambda_{S_{\text{CNT}}} \int_{W \lambda_{S_{\text{CNT}}}}^{+\infty} \frac{e^{-u}}{u} du. \quad \text{(A.11)}$$

Totally, $P_{\text{O,CNFET}}$ can be expressed as follows:

$$P_{O,\text{CNFET}} = e^{-\lambda_{S_{\text{CNT}}} W} - W \lambda_{S_{\text{CNT}}} \left(\Gamma(0, W \lambda_{S_{\text{CNT}}}) \right) \quad \text{(A.12)}$$

where Γ is the incomplete gamma function [20].

In order to investigate the efficiency of the proposed compact model, we conduct some studies where $P_{\text{O,CNFET}}$ is estimated using a Monte–Carlo (MC) simulation approach. The simulation is run by considering 1200 length intervals which are randomly placed on AFM images of CNTs. In each study, the length of intervals is set equal to the CNFET width. The failure probability is computed by the number of intervals which do not cross any CNT, divided by the total number of intervals. Table II indicates that there is only a negligible error in the statistical estimation comparing to MC simulation.

The derivation of $P_{\text{O,CNFET}}$ is related to all CNTs, regardless of their types (s- or m-CNTs). For short defects, the spacing between m-CNTs must be modeled, and thus the distribution of m-CNT spacing is of interest. We derive such distributions by assuming that the probability of any CNT being an m-CNT (s-CNT) is $P_m (P_s)$, independent of the types of its neighboring CNTs [21], with $P_m + P_s = 1$.

Consider the spacing between two m-CNTs separated by a random number of s-CNTs. We label the first m-CNT as CNT_0 and the subsequent m-CNT as CNT_K (with K-1 s-CNTs between the two m-CNTs). Then, according to the above assumption, K is a geometrically distributed random variable [22]. The spacing between two m-CNTs can be modeled by the following stochastic sum of the original spacing distribution:

$$\mathbb{S}_{m-\text{CNT}} = \sum_{i=1}^{K} S_{\text{CNT},i} \text{ with } \mathbb{K} \sim Geomentric(P_m) \quad \text{(A.13)}$$

where $S_{\text{CNT,i}}$ is a random variable that refers to the CNT pacing between CNT_i and CNT_{i+1}. In general, this distribution can be derived from the moment generating function of a random variable according to the Erlang distribution function [19] with parameter $(\lambda_{s\text{CNT}}, \mathbb{K})$, where $\mathbb{K}$ follows a geometric distribution. However, the derivation of this distribution is complicated and out of the scope of this paper. In order to make the analysis more tractable, we approximate the distribution of $\mathbb{S}_{\text{m}-\text{CNT}}$ using an exponential distribution function

$$\mathbb{S}_{m-\text{CNT}} \sim \text{Exponential}(\lambda_{S_{m-\text{CNT}}}) \quad \text{(A.14)}$$

where $\lambda_{S_{m-\text{CNT}}}$ is the distribution parameters of m-CNT spacing, which will be calculated as explained next.

As CNTs are grown chemically and in a bottom-up process, the location of each CNT is independent of those of other CNTs [12]. As a result, we can assume that all CNT spacing random variables, $S_{\text{CNT},i}$ $i = 1, 2, \ldots, K$, are identical and independently distributed. So, considering (A.13), we can write

$$\mathbb{S}_{m-\text{CNT}} = \sum_{i=1}^{\mathbb{K}} S_{\text{CNT},i} = \mathbb{K}\mathbb{S}_{\text{CNT}}. \quad \text{(A.15)}$$

Based on the moment generation function definition [19], the first moment generation function of $\mathbb{S}_{\text{m}-\text{CNT}}$, $E(\mathbb{S}_{\text{m}-\text{CNT}})$,

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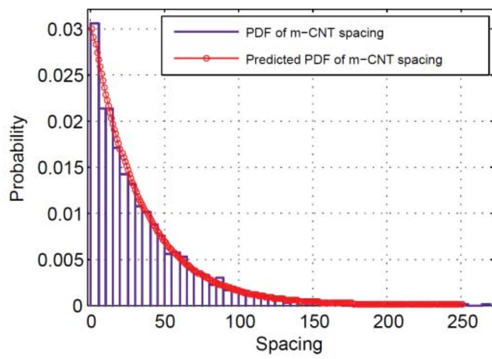

Fig. 17. Comparison of experimentally extracted distribution of m-CNT spacing with predicted statistical distribution of m-CNT spacing.

is calculated by

$$E(\mathbb{S}_{\text{m}-\text{CNT}}) = E(\mathbb{K}\mathbb{S}_{\text{CNT}}). \tag{A.16}$$

Since the distributions of $\mathbb{K}$ and $\mathbb{S}_{\text{m}-\text{CNT}}$ are independent, the $\mathbb{S}_{\text{m}-\text{CNT}}$ distribution parameter, $\lambda_{\text{Sm}-\text{CNT}}$, can be derived by

$$E(\mathbb{S}_{\text{m}-\text{CNT}}) = E(\mathbb{K})E(\mathbb{S}_{\text{CNT}}). \tag{A.17}$$

Considering the first moment generation function of exponential distribution and (A.17), the $\mathbb{S}_{\text{m}-\text{CNT}}$ distribution parameter, $\lambda_{\text{Sm}-\text{CNT}}$, can be calculated as follows:

$$\frac{1}{\lambda_{s_{\text{m}-\text{CNT}}}} = \frac{1}{P_m} \times \frac{1}{\lambda_{s_{\text{CNT}}}} \Rightarrow \lambda_{s_{\text{m}-\text{CNT}}} = P_m \lambda_{s_{\text{CNT}}}. \tag{A.18}$$

Fig. 17 shows the experimental m-CNT spacing distribution for $P_m = 0.3$ along with the predicted distributions derived by exponential approximation in (A.14). As Fig. 17 shows, the prediction gives similar results when compared with the experimentally extracted distribution. As a result, the exponential approximation is appropriate for practical cases.

To derive the short defect failure probability, we take an example of a short defect in a CNFET shown in Fig. 18. First, we consider the case in which the left side of the CNFET is placed in the right side of an m-CNT by an infinitesimal amount [Fig. 18(a)]. We name this m-CNT as m-CNT$_L$ and the nearest m-CNT placed in the right side of m-CNT$_L$ as m-CNT$_{L+1}$ (Fig. 18). In this case, if W is greater than the spacing between m-CNT$_L$ by m-CNT$_{L+1}$ ($S_{\text{m}-\text{CNT}}$), there will be at least one m-CNT in the active region of CNFET leading to a short defect. As a result, the short failure probability is equal to the probability that $\mathbb{S}_{\text{m}-\text{CNT}}$ is less than W

$$P_{\text{S,CNFET}} = P(W \geq \mathbb{S}_{\text{m}-\text{CNT}}). \tag{A.19}$$

In reality, the left side of the CNFET may be at any random position with equal probability for all positions between m-CNT $_L$ and m-CNT$_{L+1}$. As a result, the distribution of the spacing between the left side of the CNFET and the m-CNT$_L$, denoted by S_{m0}, can be approximated by a continuous uniform distribution with parameters 0 and $S_{\text{m}-\text{CNT}}$. In this case, if the value of $S_{m0}+W$ is greater than $S_{\text{m}-\text{CNT}}$, there will be at least one m-CNT in the active region leading to a short defect. Thus, the short failure probability can be expressed as follows:

$$P_{\text{S,CNFET}} = P(\mathbb{S}_{m0} + W \geq \mathbb{S}_{\text{m}-\text{CNT}}). \tag{A.20}$$

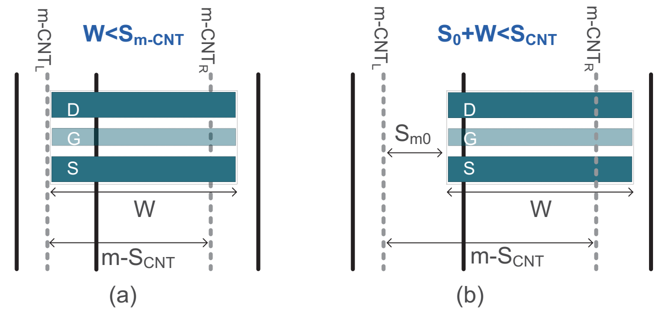

Fig. 18. Short defect in a CNFET. (a) m-CNT$_L$ is placed on the left side of CNFET. (b) There is a distance, S$_{m0}$, between m-CNT$_L$ and the left side of CNFET.

Using a similar approach to the open failure probability derivation, the short failure probability of a CNFET can be approximated as follows:

$$P_{\text{S,CNFET}} = 1 - \left(e^{-\lambda_{\text{m}-\text{CNT}}W} - W\lambda_{\text{m}-\text{CNT}}\left(\Gamma\left(0, W\lambda_{\text{m}-\text{CNT}}\right)\right)\right). \tag{A.21}$$

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