Layout Characterization and Power Density Analysis for Shorted-Gate and Independent-Gate 7nm FinFET Standard Cells

Tiansong Cui, Bowen Chen, Yanzhi Wang, Shahin Nazarian and Massoud Pedram
University of Southern California
Los Angeles, CA, USA
{tcui, bowenche, yanzhiwa, shahin, pedram}@usc.edu

ABSTRACT

In this paper, a power density analysis is presented for 7nm FinFET technology node based on both shorted-gate (SG) and independent-gate (IG) standard cells operating in multiple supply voltage regimes. A Liberty-formatted standard cell library is constructed by selecting the appropriate number of fins for the pull-up and pull-down networks of each logic cell. Next, each cell is characterized by doing SPICE simulations to calculate the propagation delays and output transition times as a function of input transition times and load capacitance values. Finally, the power density of 7nm FinFET technology node is analyzed and compared with the 45 nm CMOS technology node for different circuits. Experimental result shows that the power density of each 7nm FinFET circuit is 3-20 times larger than that of 45nm CMOS circuit under the spacer-defined technology. Experimental result also shows that the back-gate signal enables a better control of power consumption for independent-gate FinFETs.

Categories and Subject Descriptors

B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

Keywords

FinFET; Layout; Power Density; Independent Gate Control

1. INTRODUCTION

Thermal effect has gained growing attention to VLSI designers due to the increasing packing density and power consumption of VLSI circuits [1]. The need to reduce the power consumption of digital circuits in order to meet thermal constraints has caused aggressive voltage scaling from the traditional super-threshold regime to the near/sub-threshold regime[2][3]. In addition, with the dramatic downscaling of layout geometries, the traditional bulk CMOS technology is facing significant challenges due to several reasons such as the increasing leakage power and short-channel effects (SCEs) [4]. FinFET devices, a special kind of quasi-planar double gate devices, have attracted a lot of attention as an alternative to the bulk CMOS when technology scales beyond the 32nm technology node, owing to their superior performance [5][6], better scalability [7], lower leakage [8], and stronger immunization to process variations [9].

GLSVLSI'15, May 20–22, 2015, Pittsburgh, PA, USA.

http://dx.doi.org/10.1145/2742060.2742093.

Due to the promising future of the nanoscale FinFET devices, considerable research efforts have been made to study their models and characteristics. Among all of them, a unique feature of FinFET devices is the independent gate control, i.e., the front gate and the back gate can be controlled by separate signals, which enables more flexible circuit designs [10]. Due to the capacitor coupling of the front gate and the back gate, the threshold voltage of the front-gate-controlled FET varies in response to the back gate biasing, and vice versa [11]. Previous work [12] utilized the independent gate control for FinFETs in the pull-down network of an SRAM cell to keep the $20\,pA/\mu m$ standby power budget, whereas the authors of [13] studied joint gate sizing and negative biasing on the back gate of FinFET devices and demonstrated significant power reduction.

Although the fabrication and application of independent gate control in FinFET devices have been well researched, none of the previous works have focused on the thermal-effect analysis caused by independent gate control, especially for future ultra-scaled FinFETs. Considering that power-density has a strong and direct impact on the thermal characteristics of VLSI circuits, we present a power density analysis for 7nm FinFET technology node operating in super-threshold and near-threshold operation regimes, including both shorted-gate (SG) and independent-gate (IG) devices based on a created Liberty-formatted standard cell library [**?**]. For each logic cell in this library, we select the appropriate number of fins for the pull-up and pull-down networks, calculate the delay and power parameters, and then use the lambda-based layout design rules to characterize the FinFET cell layout. All cell layouts are designed using the same height to help with floorplanning flexibility, cell interconnection, and eventually area reduction. Finally, the power density of the 7nm FinFET technology node is analyzed and compared with the state-of-the-art 45nm CMOS technology node for different ISCAS benchmarks by calculating the ratio of total power consumption and estimated area. Experimental results confirm that the power density of a circuit in 7nm FinFET node can be at least 3 to 20 times larger than that in 45nm CMOS node under the spacer-defined technology. In addition, we also apply different voltage levels to the back-gate signal of the independent-gate cells. It shows that the back-gate signal enables a better control of power consumption for independent-gate FinFETs.

The rest of this paper is organized as follows. Section 2 introduces the properties of 7nm FinFET devices including the independent gate control. Section 3 explains the library format and characterization flow. The layout characterization details are elaborated in Section 4. We show the synthesis results as well as the power density reports in Section 5 and conclude the paper in Section 6.

2. BACKGROUND

FinFET devices show better suppression of the short channel effect, lower energy consumption, higher supply voltage scaling

capability, and higher ON/OFF current ratio compared with the bulk CMOS counterparts [6]. In this paper, we focus on 7nm FinFET technology node including both shorted-gate and independent-gate FinFET devices operating in both near-threshold and super-threshold supply voltage regimes. Near-threshold operation regime achieves reduced energy consumption at the cost of degradation of circuit speed. To enable both low power and high performance applications, we perform power density analysis under two supply voltages: 0.3V for near-threshold regime and 0.45V for super-threshold regime.

2.1 7nm FinFET Technology Node

The structure of a 7nm FinFET device is shown in Figure 1. The FinFET device consists of a thin silicon body with thickness of T_{fin}, which is wrapped by gate electrodes. The device is termed quasi-planar as the current flows in parallel with the wafer plane, and the channel is formed perpendicular to the plane. The effective gate length L_G is twice as large as the fin height h_{fin}. The spacer length L_{SP} is an important design parameter that directly relates to the short channel effects [14]. The FinFET structure allows for fabrication of separate front and back gates. In this structure, each fin is essentially the parallel connection of the front-gate-controlled FET and the back-gate-controlled FET, both with a width equal to the fin height h_{fin}.

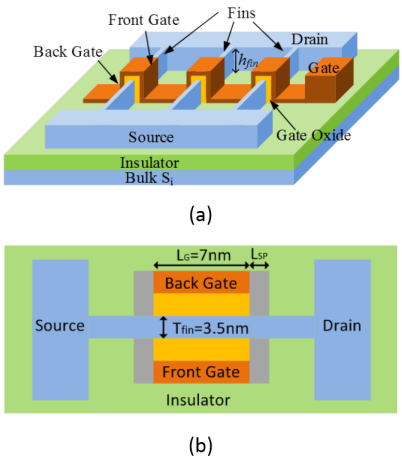

Figure 1: (a) Perspective view and (b) top view of the 7nm FinFET device.

2.2 Independent Gate Control for FinFET Devices

A unique feature of FinFET devices is the independent gate control, where the front and back gates can be tied to the same or different control signals, allowing for more flexible circuit designs. Due to capacitor coupling of the front gate and the back gate of a FinFET transistor, the threshold voltage of the front-gate-controlled FET varies in response to the back-gate voltage, and vice versa [15]. Figure 2 shows the relationship between the threshold voltage of the front-gate-controlled FET and the back-gate voltage from the Hspice simulation. Under a relatively small back-gate voltage, a linear relationship between the change of the threshold voltage of front-gate and the back-gate voltage is observed (suppose that we consider N-type FETs).

The unique feature of independent gate control is exploited in previous works [10]-[13], where different implementation modes of FinFET logic gates are proposed and applied. For the N-type or P-type fin, there are two different connection modes: (i) the shorted-gate (SG) mode, where the front gate and the back gate of the fin are tied together to the input signal, and (ii) the independent gate (IG) mode, where one of the gate is driven by the input signal

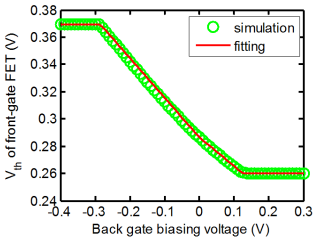

Figure 2: V_{th} of the front-gate-controlled N-type FET vs. back-gate voltage.

and the other is connected to a pre-defined biasing voltage or to the ground. For multiple-input logic cells (e.g., NAND, NOR), there is another IG mode connection where the front gate and back gate are driven by different input signals [16]. These different modes achieve a trade-off between power consumption and rise/fall delay. We illustrate in Figure 3 three examples of implementing a FinFET NAND gate.

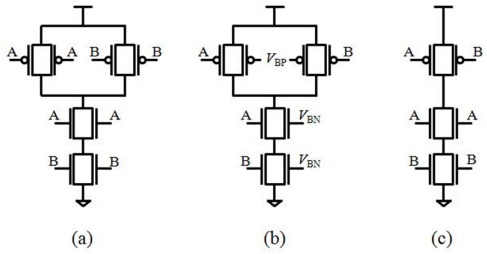

Figure 3: Different FinFET-based NAND gate designs.

In this paper, we perform power density analysis based on both shorted-gate and independent-gate 7nm FinFET standard cells. FinFETs operating designed in shorted-gate mode offer the highest driving strength [17], and we consider shorted-gate FinFETs operating in both near-threshold and super-threshold regimes. On the other hand, independent-gate FinFETs are often used in low power implementations, where a reverse-biasing voltage (i.e., the biasing voltage is low for nFETs and high for pFETs) is used to reduce subthreshold leakage [17]. As a result, we consider independent-gate FinFETs operating in only near-threshold regime, but apply different biasing voltage levels.

3. 7NM FINFET STANDARD CELL LIBRARY CHARACTERIZATION

The main goal of this paper is to perform thermal analysis on a given FinFET circuit, which requires the gate-level implementation of the circuit (in shorted-gate mode or independent-gate mode) and thus the characterization of standard cell library is needed. A standard cell library is a set of high-quality timing and power models that accurately and efficiently capture the behavior of standard cells. The standard cell library is widely used in many design tools for different purposes, such as logic synthesis, static timing analysis, power analysis, high-level design language simulation, and so on, as part of Computer-Aided-Design (CAD). The Liberty library format (.lib), which was first invented by Synopsys a decade ago, has become an industrial standard that is adopted by over 100 semi-conductor vendors and implemented in over 75 production electronic design automation (EDA) tools [**?**]. Therefore, we build our 7nm FinFET standard cell library in the .lib format. The two major steps of building this library are standard cell sizing and power/timing parameter characterization.

Table 1: Summary of logic cells included in 7nm FinFET standard cell library

Logic Cell	SG Scale	IG Scale
Inverter	1X, 2X, 4X, 8X	1X, 2X
2-input NAND	1X, 2X, 4X, 8X	1X
3-input NAND	1X, 2X, 4X	1X
2-input NOR	1X, 2X, 4X, 8X	1X
3-input NOR	1X, 2X, 4X	1X
AND-OR-INV	1X, 2X, 4X	1X
OR-AND-INV	1X, 2X, 4X	1X
XOR	1X, 2X	1X
XNOR	1X, 2X	1X
MUX	1X, 2X	1X
Latch	1X	1X
D-flip-flop	1X	1X
D-flip-flop w/ S/R	1X	1X

3.1 Standard Cell Sizing

The driving strength of a short-gate or independent-gate FinFET device depends on the ratio of fin height and channel length, while both parameters are determined by the fabrication technology. Thus, the FinFET standard cell sizing involves selecting the appropriate number of fins for the pull-up network and pull-down network of each logic cell. The general sizing method is to balance the rise and fall delays of a standard cell. We first investigate the numbers of P-type fins and N-type fins in an inverter that achieve approximately equal rise and fall delays. According to the transregional FinFET model [18], the drain current of a FinFET in the sub- and near-threshold regimes is given by

$$I_{ds} = I_0 e^{\frac{(V_{gs}+\lambda V_{ds}-V_{th})-\alpha(V_{gs}+\lambda V_{ds}-V_{th})^2}{m \cdot v_T}} (1 - e^{\frac{-V_{ds}}{v_T}}) \quad (1)$$

where λ is the drain voltage dependency coefficient (similar to but much smaller than the DIBL coefficient for bulk CMOS devices), v_T is the thermal voltage, and I_0, α, and m are technology-dependent parameters to be derived using Hspice simulation. In order to achieve equal rise and fall delay, the number of P-type fins N_P in an inverter can be determined by

$$N_P = N_N \cdot \frac{I_{ds,N}}{I_{ds,P}} \quad (2)$$

where $I_{ds,N}(I_{ds,P})$ is the drain current of an N-type(P-type) fin when $|V_{gs}| = |V_{ds}| = V_{DD}$, and N_N is the number of N-type fins in the inverter. Based on equation (2) and Hspice simulation, the N_P/N_N ratio can be determined for different size of inverters. We observe that the driving strengths of P-type and N-type fins are balanced for both shorted-gate and independent-gate FinFET inverters using the same size.

We also use the method described in [18] to solve the stack sizing problem and design other combinational and sequential logic cells in near-threshold regime. All the logic cells included in the 7nm FinFET standard cell library are summarized in Table 1. Please note that: (i) For shorted-gate cells, we use the same sizing of FinFET logic cells in the super-threshold regime ($V_{DD} = 0.45V$), since we assume our standard cells support DVFS (dynamic voltage and frequency scaling); (ii) As independent-gate logic cells are designed for low-power use, we include only 1X and 2X scales for inverter and 1X scale for all the other cells.

3.2 Power/Timing Parameter Characterization

When the number of fins of each standard cell is determined, the timing parameters and power parameters need to be calculated and stored in 2D look-up-tables (LUTs) in the input/output pin-level [**?**]. We obtain the timing and power parameters of each logic cell of interest through Hspice simulations at various input and output conditions based on the Verilog-A based 7nm FinFET device model. The timing parameters of a logic cell refer to propagation delays and transition times of the output pin when the output makes a transition. For sequential cells such as D flip-flops and latches, the timing parameters also include time check parameters such as the setup time and hold time of the data signal, and the recovery time and removal time of asynchronous control signals. The propagation delays and transition times are represented by using 2D LUTs, which are indexed by input transition times and capacitive load at the output pin. The power parameters in the Liberty library include the leakage power and internal power of a logic cell. The overall power consumption is evaluated by summing up the leakage power, internal power, and switching power (power consumed when charging and discharging the capacitive load). The internal power accounts for the short-circuit power consumption and dynamic power of the diffusion capacitors at the output pin of the logic cell. Also 2D LUTs are used to store internal power values of the output pin related to each input pin. Detailed characterization steps are omitted in this paper because of space limit.

4. 7NM FINFET STANDARD LAYOUT CHARACTERIZATION

The standard cell library characterization enables synthesis and total power estimation of a certain circuit. In order to analyze the power density of 7nm FinFET technology, we also estimate the total area consumption of a given circuit by designing the layout of each cell based on the lambda-based layout design rules for FinFET devices. In this section, we present the layout of each standard cell based on the sizing result of the previous section, including both shorted-gate and independent-gate cells. Our FinFET layout design rules also consider the interconnection between different cells.

4.1 FinFET Layout Design Rules

General understanding of the FinFET layout density is challenged by its dependence on the specific technology adopted to manufacture the "fin" (which is the core of FinFET) [19]. Figure 4 shows the comparison between the layout of a general CMOS device and a shorted-gate FinFET device with four fins. In this FinFET layout structure, a single strip is used for the gate terminal, while source and drain terminals of multiple fins are connected together through a metal wire to make a wider FinFET device. This is different from CMOS devices.

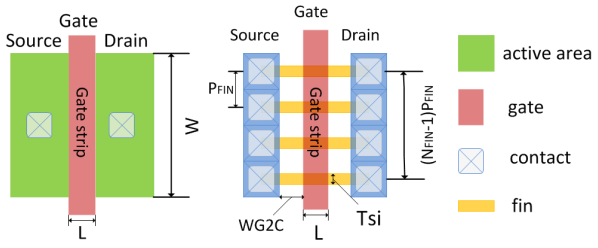

Figure 4: Layout of (a) a general CMOS device and (b) a shorted gate FinFET device with four fins.

In this section, we used the modified lambda-based layout design rules to characterize the layout of each FinFET logic cell. Authors in [20] have reported the major process-related FinFET geometries for 5nm technology and similar values can be derived for 7nm technology, which is shown in Table 2. The detailed process design rules are also included in this table. Notice that generally the layout design rules are similar for CMOS and FinFET technologies because the major difference is on fin fabrication [21]. One critical process-related geometry for FinFET devices shown in Figure 4 is the fin pitch, P_{FIN}, which is defined as the minimum center-to-center distance of two adjacent parallel fins. The value of P_{FIN} is determined by the underlying FinFET technolo-

gy. More precisely, there are two types of FinFET technologies: (1) lithography-defined technology where lithographic constraints limit the fin pitch spacing, and (2) spacer-defined technology which relaxes the constraints on P_{FIN}, and obtains 2x reduction in the value of P_{FIN} at the cost of a more elaborate and costly lithographic process [22]. In this paper, we focus on the layout characterization of 7nm spacer-defined technology in order to perform a pessimistic estimation on power density in 7nm FinFET technology node.

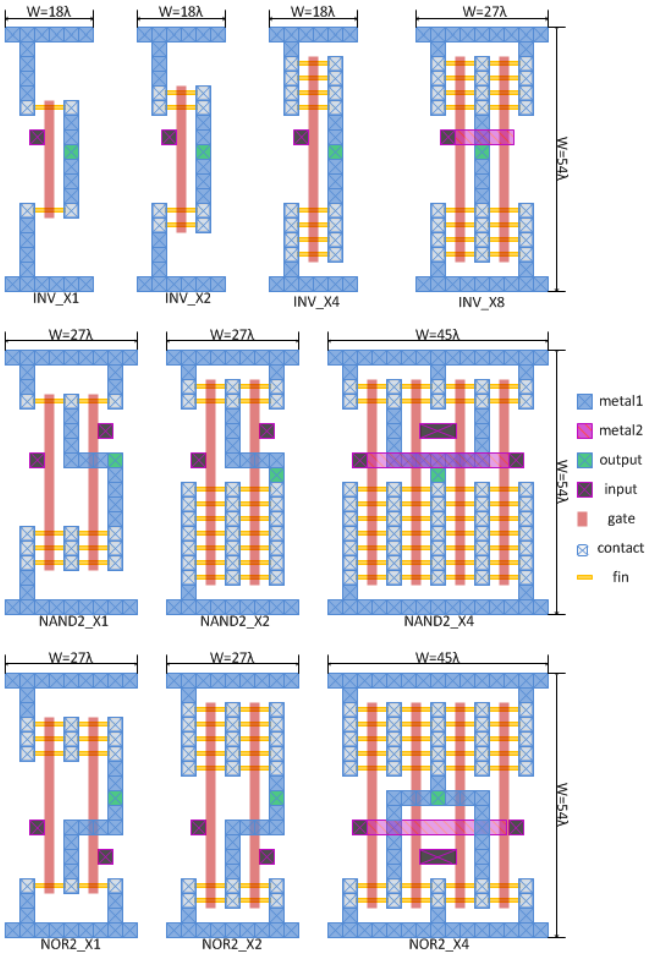

Figure 5: 7nm FinFET shorted-gate layout of inverters, 2-input NAND gates and 2-input NOR gates with different sizes

4.2 7nm FinFET Shorted-Gate Standard Cell Layout

Based on FinFET-specific geometries and design rules, the layouts of shorted-gate standard cells can be determined according to the sizing results of each logic cell, which has been shown in Section 3.1. To achieve higher layout flexibility, the number of fins for certain cells has been slightly adjusted. In addition, considering both area consumption and floorplanning flexibility, all the standard cell layouts are designed with the same height. We set the height of all the cells the same as the standard 2-input 2X NAND (equivalently 2X NOR and 4X inverter) cell in order to achieve the best tradeoff between design flexibility and area waste. These three types of cells occupy over 40% of the total number of cells based on our experimental result for different ISCAS benchmarks, and we have verified that using these three types of cells to determine the standard height will achieve the smallest total area consumption for ISCAS circuits. The shared diffusion and width extension can be used when we design the layout of larger cells. Figure 5 shows the layout geometry of some basic cells with different sizes. In our standard cell library, all the gates are designed with a fixed height of 54λ. Inverter 1X, 2X and 4X gates achieve an active width of 27λ and the 2-input NAND gates of both 1X and 2X sizes have an active width of 27λ. The 8X inverter and 2-input 4X NAND gate have active widths of 27λ and 45λ respectively by using shared diffusion and width extension. 2-input NOR gate has the same area consumption as 2-input NAND gate of the corresponding size. Notice that the active width has already included the layout interconnect overhead, which is shared by 6λ per cell.

Table 2: FinFET-specific geometries and design rules

Parameter	Value in 7nm FinFET (nm)	Value in 5nm FinFET (nm)	Comment
L_{FIN}	$2\lambda = 7$	$2\lambda = 7$	Fin length
T_{SI}	3.5	2.725	Fin width
H_{FIN}	14	10.9	Fin height
P_{FIN}	$3\lambda = 10.5$	$3\lambda = 7.5$	Fin pitch using spacer lithography
t_{ox}	1.55	1.09	Oxide thickness
W_C	$3\lambda = 10.5$	$3\lambda = 7.5$	Minimum contact size
W_{M2M}	$3\lambda = 10.5$	$3\lambda = 7.5$	Minimum space between metal wires
W_{G2C}	$2\lambda = 7$	$2\lambda = 5$	Minimum space of gate to contact

4.3 7nm FinFET Independent-Gate Standard Cell Layout

The introduction of the independent-gate FinFET brings more associated design rules. After the separation of the gate electrodes, each gate segment must be contacted electrically [23]. Therefore, a contact must be placed on the gate poly line between each pair of fins. A major design rule affecting the IG FinFET layout is the "CA over PC to RX" rule [23]. This rule adds a space of W_{M2M} to the distance between two adjacent fins in order to place a contact on every gate segment between every pair of fins, as seen in Figure 6.

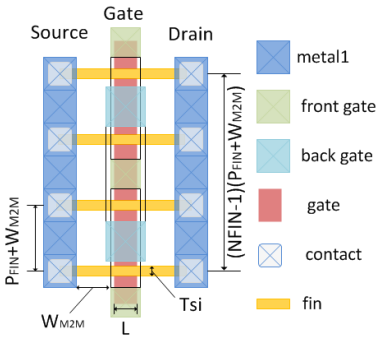

Figure 6: Layout of an independent gate FinFET device with four fins.

The layout of independent-gate standard cells is shown in Figure 7. To maintain the compatibility of FinFET standard cells in different modes, all the IG standard cell layouts are designed with the same height of SG standard cells. In addition, considering that the back-gate control (for Pfet or Nfet) is a kind of global signal, we align the back-gate control signals of different standard cells in order to make it easier for interconnection. The width of IG standard cell turns out to be a little wider than the SG standard cell of the same size.

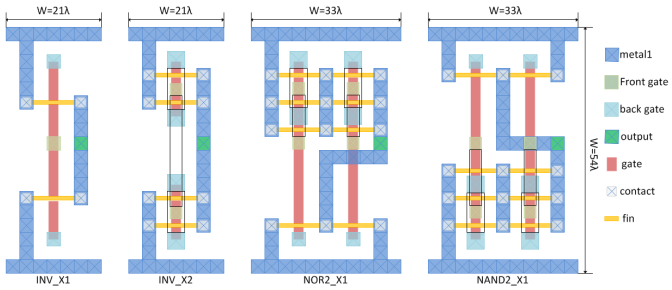

Figure 7: 7nm FinFET independent-gate layout of inverters, 2-input NAND gates and 2-input NOR gates

Table 3: 7nm FinFET Standard Cell Layout Geometries

Cell Type	SG Active Width (λ)	IG Active Width (λ)
Inverter	18, 18, 18, 27	21, 21
2-input NAND	27, 27, 45, 81	33
3-input NAND	36, 63, 117	45
2-input NOR	27, 27, 45, 81	33
3-input NOR	36, 63, 117	45
AND-OR-INV	36, 63, 117	45
OR-AND-INV	36, 63, 117	45
XOR	60, 87	77
XNOR	60, 87	77
MUX	81, 129	105
Latch	90	117
D-flip-flop	156	205
D-flip-flop w/ S/R	192	253

According to the FinFET-specific layout design rules as well as our fixed-height design method, the layout of combinational logic cells and the sequential logic cells can be derived accordingly. The geometries of all the logic cells included in the 7nm FinFET standard cell library are summarized in Table 3.

5. EXPERIMENTAL RESULT AND POWER DENSITY ANALYSIS

To predict the power density values in 7nm FinFET technology, we synthesize various ISCAS benchmark circuits using the developed FinFET standard cell library for both shorted gate mode (in super-threshold regime and near-threshold regime) and independent-gate mode (in near-threshold regime). The power density value is calculated as the ratio of power consumption and the total area of the circuit. We use 45nm CMOS technology for comparison because there are widely-received libraries and thermal analysis results in this technology node. The same circuits are synthesized using the 45nm CMOS library developed by North Carolina State University (NCSU). All benchmark circuits are synthesized by Synopsys Design Compiler.

In order to estimate the power consumption of each circuit in reality, we assume the circuit is operating in a processor with a frequency of f and also we consider an activity factor α, which determines the circuit switching activity. The average power consumption of a circuit can be calculated using:

$$P_{average} = P_{leakage} + \alpha \cdot P_{dynamic} \cdot D \cdot f, \qquad (3)$$

where both the leakage power $P_{leakage}$ and the dynamic power $P_{dynamic}$ can be found in the power report from Design Compiler. The value D in this equation represents the circuit delay (which can be found in the timing report) and thus $P_{dynamic} \cdot D$ is the average energy consumption per clock cycle (in other words the average energy consumed inside a circuit when it operates on a new input value). In this paper, the α value is set to be 0.2 and we assume the circuit is operating under a frequency of 500Mz when estimating the average power consumption. Our estimated power density of 45nm CMOS technology matches the previously reported value, which is around $140mW/mm^2$ [24].

We first analyze the power density comparison between 7nm FinFET shorted-gate circuit and 45nm CMOS circuit for different ISCAS benchmarks, which is summarized in Table 4. One can observe that the power density of 7nm FinFET SG circuits can reach over $1500mW/mm^2$ in near-threshold regime and over $2500mW/mm^2$ in super-threshold regime. These values are much higher than the limit of air cooling (around $1000mW/mm^2$ [25]) and careful thermal management will be needed for FinFET devices operating in shorted-gate mode. Notice that the power density in 7nm FinFET technology can be even higher than these values, because we assume the operating frequency is the same for 45nm CMOS and 7nm FinFET technologies, while in reality, FinFET circuits achieve a much better delay and thus the operating frequency can be higher than that of 45nm CMOS circuits [14].

We also apply different back-gate voltage levels to 7nm IG FinFET circuits, and Table 5 summarizes the power density values of IG FinFET designed ISCAS benchmarks. The reverse biasing voltage level V_{bias} is set to be 0.05V, 0V and -0.05V. We apply V_{bias} to the back-gate voltage of nFETs while the back-gate voltage of pFETs is connected to a voltage level of $(V_{dd} - V_{bias})$. It can be observed that IG FinFET circuits achieve much lower power density values compared with DG FinFET circuits, but even the lowest power density of IG FinFET circuits is still 3 times larger than that of the 45nm CMOS circuit. In addition, the power consumption (as well as the power density) for independent-gate FinFETs can be effectively controlled by the voltage level of V_{bias} because back-gate biasing voltage has an impact on the threshold voltage of the front-gate, which will then affect both dynamic power and leakage power consumption. However, the circuit performance will also be degraded when we reduce the voltage level of V_{bias}. In real FinFET circuit design, we might need to find a suitable V_{bias} level in order to achieve an optimal tradeoff between power density and circuit performance.

Notice that the layouts of shorted-gate and independent-gate FinFET standard cells are designed to be compatible with each other. One might include both SG and IG FinFET standard cells in the library of synthesis, which will result in a circuit with both shorted-gate and independent-gate FinFET devices. The power density of this circuit will be between that of the corresponding pure SG FinFET circuit and pure IG FinFET circuit.

6. CONCLUSION

Nanoscale FinFET devices are emerging as the transistor of choice because they allow for higher voltage scalability and design flexibility. In this paper, we present a power density analysis for 7nm FinFET devices under multiple supply voltage regimes, including shorted-gate and independent-gate standard cells and considering both high performance and low power usage. A Liberty-formatted standard cell library is built and the layout of each cell is characterized based on the lambda-based layout design rules for FinFET devices. Finally, the power density of 7nm FinFET technology node is analyzed and compared with the advanced 45nm CMOS technology node for different circuits. It has been confirmed that under spacer-defined technology, the power density of each 7nm FinFET circuit is about 3 to 20 times larger than that of the same circuit in 45nm CMOS node. We have also shown that the back-gate signal enables a better control of power consumption as well as power density for independent-gate FinFETs.

7. ACKNOWLEDGMENTS

This research is sponsored in part by grants from the PERFECT program of the Defense Advanced Research Projects Agency.

Table 4: Power density analysis for 7nm shorted-gate FinFET and 45nm CMOS circuits

Circuit	FinFET 7nm V_{dd}=0.3V			FinFET 7nm V_{dd}=0.45V			NCSU CMOS 45nm V_{dd}=1.1V		
	Average power (μW)	Total area (μm^2)	Power density (mW/mm^2)	Average power (μW)	Total area (μm^2)	Power density (mW/mm^2)	Average power (μW)	Total area (μm^2)	Power density (mW/mm^2)
c432	9.32	6.76	1380	12.7	5.96	2131	78.9	625	126.3
c499	21.72	17.3	1256	30.8	12.4	2484	78.7	922.8	85.3
c880	11.6	15.3	757	18.9	8.93	2114	74.5	889	83.8
c1355	25.3	20.4	1241	31.3	12.2	2562	117.8	1167	100.9
c1908	26.0	15.3	1702	38.8	16.1	2410	106.9	993.1	107.7
c3540	53.5	35.6	1503	87.7	33.8	2591	396	2768	143

Table 5: Power density analysis for 7nm independent-gate FinFET circuits under V_{dd}=0.3V

Circuit	IG FinFET V_{bias}=0.05V			IG FinFET V_{bias}=0V			IG FinFET V_{bias}=-0.05V		
	Average power (μW)	Total area (μm^2)	Power density (mW/mm^2)	Average power (μW)	Total area (μm^2)	Power density (mW/mm^2)	Average power (μW)	Total area (μm^2)	Power density (mW/mm^2)
c432	4.87	5.06	961	2.88	5.06	569.6	2.28	5.06	450.8
c499	6.95	9.86	705	4.11	9.86	417.3	3.26	9.86	330.2
c880	7.72	13.9	557	4.57	13.9	330.0	3.62	13.9	261.1
c1355	5.85	9.4	623	3.47	9.4	368.7	2.74	9.4	291.8
c1908	8.71	11.4	762	5.16	11.4	451.1	4.08	11.4	356.9
c3540	34.1	29.9	1143	20.2	29.9	677.1	16.0	29.9	535.8

8. REFERENCES

[1] M. Pedram and S. Nazarian, "Thermal modeling, analysis, and management in vlsi circuits: Principles and methods," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1487–1501, 2006.

[2] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming moore's law through energy efficient integrated circuits," *Proceedings of the IEEE*, vol. 98, no. 2, pp. 253–266, 2010.

[3] D. Markovic, C. C. Wang, L. P. Alarcon, T.-T. Liu, and J. M. Rabaey, "Ultralow-power design in near-threshold region," *Proceedings of the IEEE*, vol. 98, no. 2, pp. 237–252, 2010.

[4] L. Chang, Y.-k. Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, C. Hu, and T.-J. King, "Extremely scaled silicon nano-cmos devices," *Proceedings of the IEEE*, vol. 91, no. 11, pp. 1860–1873, 2003.

[5] S. Chaudhuri and N. K. Jha, "Finfet logic circuit optimization with different finfet styles: Lower power possible at higher supply voltage," in *VLSI Design and 2014 13th International Conference on Embedded Systems, 2014 27th International Conference on*. IEEE, 2014, pp. 476–482.

[6] T. Sairam, W. Zhao, and Y. Cao, "Optimizing finfet technology for high-speed and low-power design," in *Proceedings of the 17th ACM Great Lakes symposium on VLSI*. ACM, 2007, pp. 73–77.

[7] C. H. Wann, K. Noda, T. Tanaka, M. Yoshida, and C. Hu, "A comparative study of advanced mosfet concepts," *Electron Devices, IEEE Transactions on*, vol. 43, no. 10, pp. 1742–1753, 1996.

[8] L. Chang, K. J. Yang, Y.-C. Yeo, Y.-K. Choi, T.-J. King, and C. Hu, "Reduction of direct-tunneling gate leakage current in double-gate and ultra-thin body mosfets," in *INTERNATIONAL ELECTRON DEVICES MEETING*. IEEE; 1998, 2001, pp. 99–102.

[9] A. R. Brown, A. Asenov, and J. R. Watling, "Intrinsic fluctuations in sub 10-nm double-gate mosfets introduced by discreteness of charge and matter," *Nanotechnology, IEEE Transactions on*, vol. 1, no. 4, pp. 195–200, 2002.

[10] A. Muttreja, N. Agarwal, and N. K. Jha, "Cmos logic design with independent-gate finfets," in *Computer Design, 2007. ICCD 2007. 25th International Conference on*. IEEE, 2007, pp. 560–567.

[11] F. Crupi, M. Alioto, J. Franco, P. Magnone, M. Togo, N. Horiguchi, and G. Groeseneken, "Understanding the basic advantages of bulk finfets for sub-and near-threshold logic circuits from device measurements," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 59, no. 7, pp. 439–442, 2012.

[12] T. Cakici, K. Kim, and K. Roy, "Finfet based sram design for low standby power applications," in *Quality Electronic Design, 2007. ISQED'07. 8th International Symposium on*. IEEE, 2007, pp. 127–132.

[13] J. Ouyang and Y. Xie, "Power optimization for finfet-based circuits using genetic algorithms," in *SOC Conference, 2008 IEEE International*. IEEE, 2008, pp. 211–214.

[14] S. K. Gupta, W.-S. Cho, A. A. Goud, K. Yogendra, and K. Roy, "Design space exploration of finfets in sub-10nm technologies for energy-efficient near-threshold circuits," in *Device Research Conference (DRC), 2013 71st Annual*. IEEE, 2013, pp. 117–118.

[15] T. Cui, Y. Wang, X. Lin, S. Nazarian, and M. Pedram, "Semi-analytical current source modeling of finfet devices operating in near/sub-threshold regime with independent gate control and considering process variation." in *ASP-DAC*, 2014, pp. 167–172.

[16] T. Cui, S. Chen, Y. Wang, S. Nazarian, and M. Pedram, "An efficient semi-analytical current source model for finfet devices in near/sub-threshold regime considering multiple input switching and stack effect," in *Quality Electronic Design (ISQED), 2014 15th International Symposium on*. IEEE, 2014, pp. 575–581.

[17] N. K. Jha and D. Chen, *Nanoelectronic Circuit Design*. springer, 2010.

[18] X. Lin, Y. Wang, and M. Pedram, "Joint sizing and adaptive independent gate control for finfet circuits operating in multiple voltage regimes using the logical effort method," in *Proceedings of the International Conference on Computer-Aided Design*. IEEE Press, 2013, pp. 444–449.

[19] M. Alioto, "Analysis of layout density in finfet standard cells and impact of fin technology," in *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*. IEEE, 2010, pp. 3204–3207.

[20] A. A. Goud, S. K. Gupta, S. H. Choday, and K. Roy, "Atomistic tight-binding based evaluation of impact of gate underlap on source to drain tunneling in 5 nm gate length si finfets," in *Device Research Conference (DRC), 2013 71st Annual*. IEEE, 2013, pp. 51–52.

[21] M. Alioto, "Comparative evaluation of layout density in 3t, 4t, and mt finfet standard cells," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 19, no. 5, pp. 751–762, 2011.

[22] Y.-K. Choi, T.-J. King, and C. Hu, "Nanoscale cmos spacer finfet for the terabit era," *Electron Device Letters, IEEE*, vol. 23, no. 1, pp. 25–27, 2002.

[23] D. M. Fried, "The design, fabrication and characterization of independent-gate finfets," Ph.D. dissertation, Cornell Unive, 2004.

[24] U. Gogineni, J. A. Del Alamo, and C. Putnam, "Rf power potential of 45 nm cmos technology," in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2010 Topical Meeting on*. IEEE, 2010, pp. 204–207.

[25] G. G. Shahidi, "Evolution of cmos technology at 32 nm and beyond," in *Custom Integrated Circuits Conference, 2007. CICC'07. IEEE*. IEEE, 2007, pp. 413–416.