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High-Level Design Challenges and Solutions for Low Power Systems

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Outline

- Introduction
- OS-Directed Power Management
- Compiler-Based Power Optimization
- Summary

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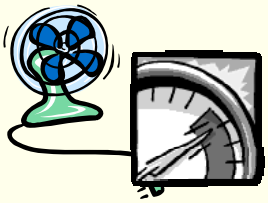
Why Low Power Design

Battery lifetime

Cooling and energy costs



Environmental concerns

System reliability

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Process Technology Trend

	1997	1999	2001	2003	2006	2009	2012
Min. Feature Size (µm)	0.25	0.18	0.15	0.13	0.1	0.07	0.05
Threshold Voltage (V)	0.5	0.45	0.4	0.35	0.3	0.25	0.2
T_{ox}(nm)	5	4	3	3	2	1.5	1
$C_{interconnect}$ (aF/µm)	50	36	29	21	20	16	14
Memory @ samples/introduction (G)	0.256	1	*	4	16	64	256
Max I_{off}(µA/µm) (For minimum L device)	1	1	3	3	3	10	10
Minimum Supply Voltage (V)	2.5	1.8	1.5	1.5	1.2	0.9	0.6
On-chip across-chip clock freq. (MHz)	400	600	700	800	1100	1400	1800
Off-chip peripheral bus freq. (MHz)	75/175	100/263	100/362	125/464	125/554	150/734	150/913
ASIC usable xtors (millions / cm^2)	8	14	16	24	40	64	100
Chip size (cm^2)	3	3.4	3.85	4.3	5.2	6.2	7.5
Chip-to-package (pad) count	800	975	1195	1460	1970	2655	3585

Cost-Perf. Designs - notebooks, desktop personal computers, telecom

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Data extracted from NTRS'97

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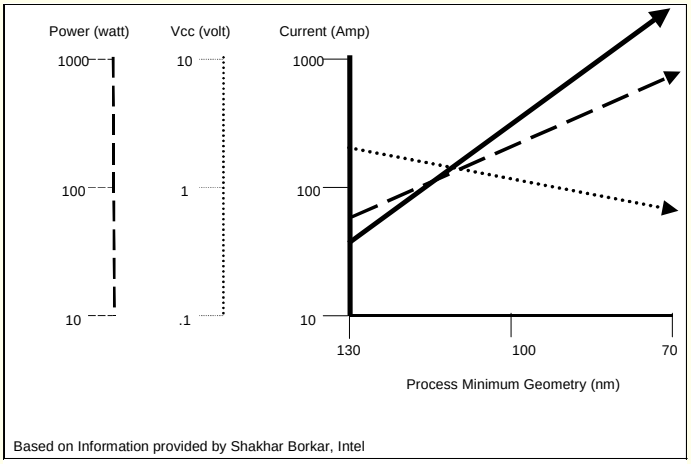
The Power Problem



Based on Information provided by Shakhar Borkar, Intel

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Data extracted from EDAR'99

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What Has Worked

- Voltage and process scaling
- Design methodologies
  - ⇨ Power-aware design flows and tools, trade area for lower power
- Architecture Design
- Power down techniques
  - ⇨ Clock gating, dynamic power management
- Dynamic voltage scaling based on workload
- Power conscious RT/ logic synthesis
- Better cell library design and resizing methods
  - ⇨ Cap. reduction, threshold control, transistor layout

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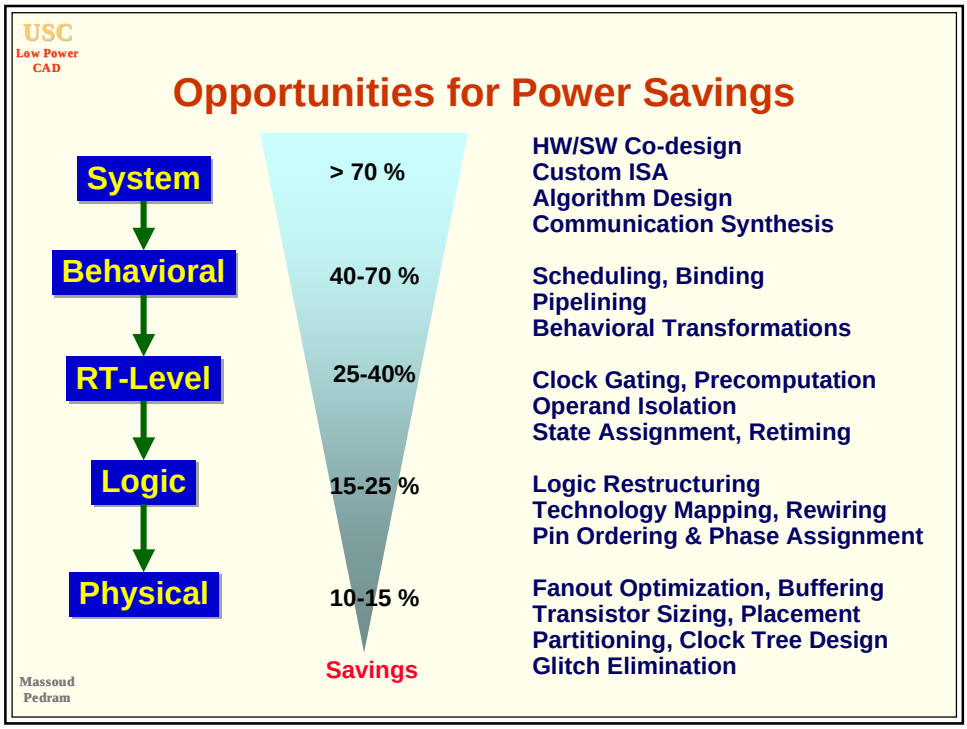
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Opportunities for Power Savings
System
Behavioral
RT-Level
Logic
Physical
> 70 %
40-70 %
25-40%
15-25 %
10-15 %
Savings
HW/SW Co-design
Custom ISA
Algorithm Design
Communication Synthesis
Scheduling, Binding
Pipelining
Behavioral Transformations
Clock Gating, Precomputation
Operand Isolation
State Assignment, Retiming
Logic Restructuring
Technology Mapping, Rewiring
Pin Ordering & Phase Assignment
Fanout Optimization, Buffering
Transistor Sizing, Placement
Partitioning, Clock Tree Design
Glitch Elimination
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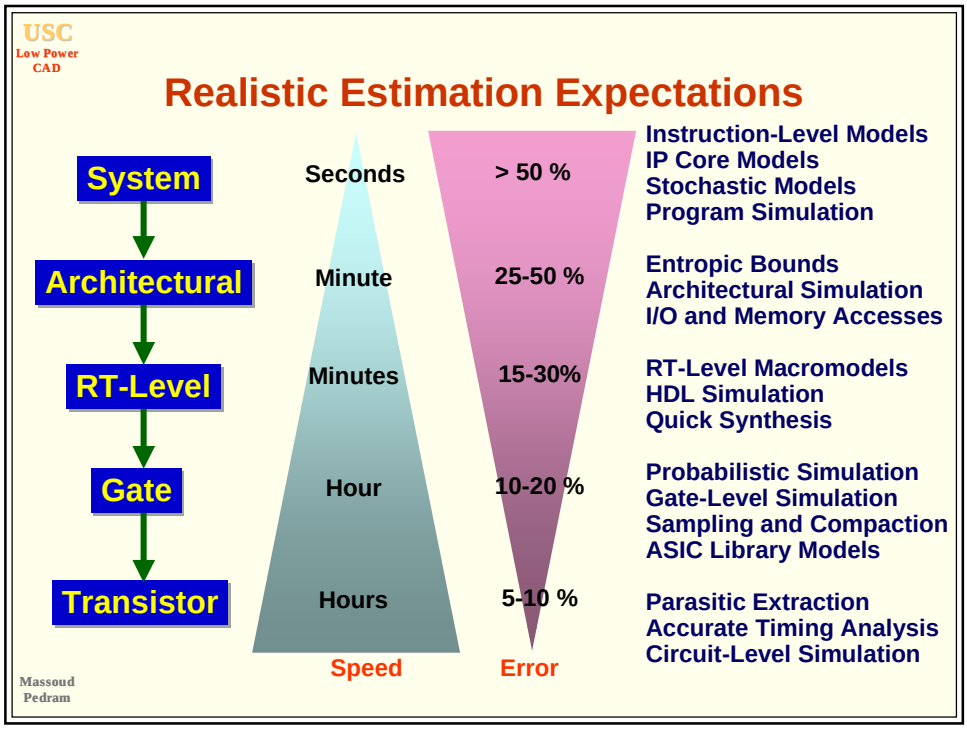
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Realistic Estimation Expectations
System
Architectural
RT-Level
Gate
Transistor
Seconds
Minute
Minutes
Hour
Hours
Speed
> 50 %
25-50 %
15-30%
10-20 %
5-10 %
Error
Instruction-Level Models
IP Core Models
Stochastic Models
Program Simulation
Entropic Bounds
Architectural Simulation
I/O and Memory Accesses
RT-Level Macromodels
HDL Simulation
Quick Synthesis
Probabilistic Simulation
Gate-Level Simulation
Sampling and Compaction
ASIC Library Models
Parasitic Extraction
Accurate Timing Analysis
Circuit-Level Simulation
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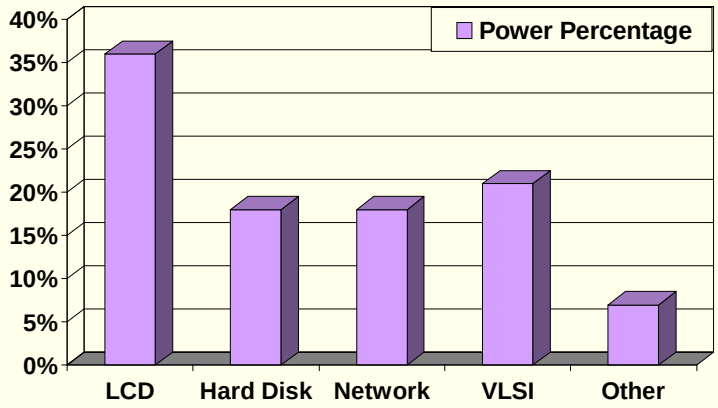
Power Control at the System Level

- Power break down in a portable computer



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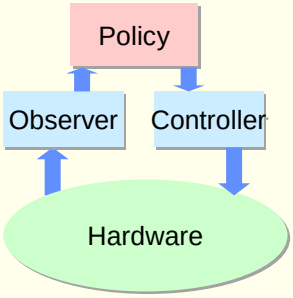
OS-Directed Power Management

- Motivations
  - ⇨ Digital circuitry has been researched a lot
  - ⇨ Idle or under-utilized resources can be shut down or slowed down
- Why use OS
  - ⇨ OS knows all activities (state of system: running, sleep or waiting
  - ⇨ Can communicate with devices
  - ⇨ Can include DPM as a module
- DPM module
  - ⇨ Observer -- collecting data from devices
  - ⇨ Policy -- decision management
  - ⇨ Controller -- steer hardware



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ACPI: An Industrial Standard

- Advanced Configuration and Power Interface (ACPI) [Intel, Microsoft, Toshiba]
- Interface between OS and hardware
- Abstract, hierarchical finite-state machine
- Each state represents power and performance levels
- Global power states:
  - ⇨ *Mechanical off*: **power failure**
  - ⇨ *Soft off*: **OS reboot needed**
  - ⇨ *Sleep*: **entire system sleep, waiting for wake-up signals**
  - ⇨ *Working*: **system is operational**
  - ⇨ *Legacy*: **backward compatability**
- Policy selection:
  - ⇨ **No concrete proposal (left to the engineer's decision)**

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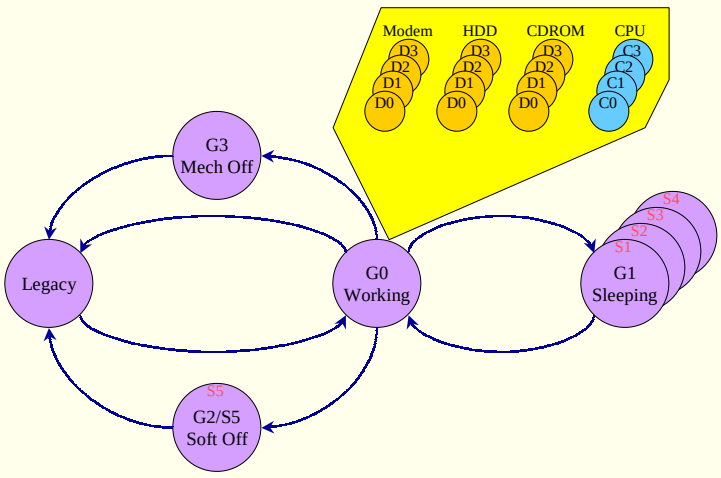
ACPI Power States



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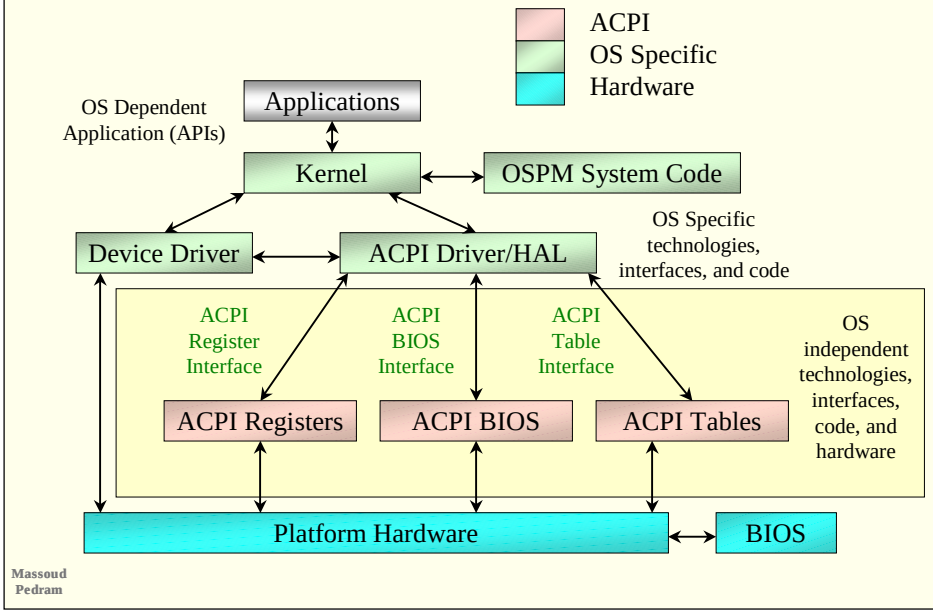
ACPI Platform



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Heuristic Approaches

- **Greedy**
  - Turn on: when SQ is not empty
  - Turn off: when SQ is empty
- **Time-out**
  - Turn on: when SQ is not empty
  - Turn off: when SQ has been empty for T seconds
- **Predictive**
  - Turn on: when SQ is not empty or at a predicted time
  - Turn off: when SQ has been empty for T seconds where T is dynamically set

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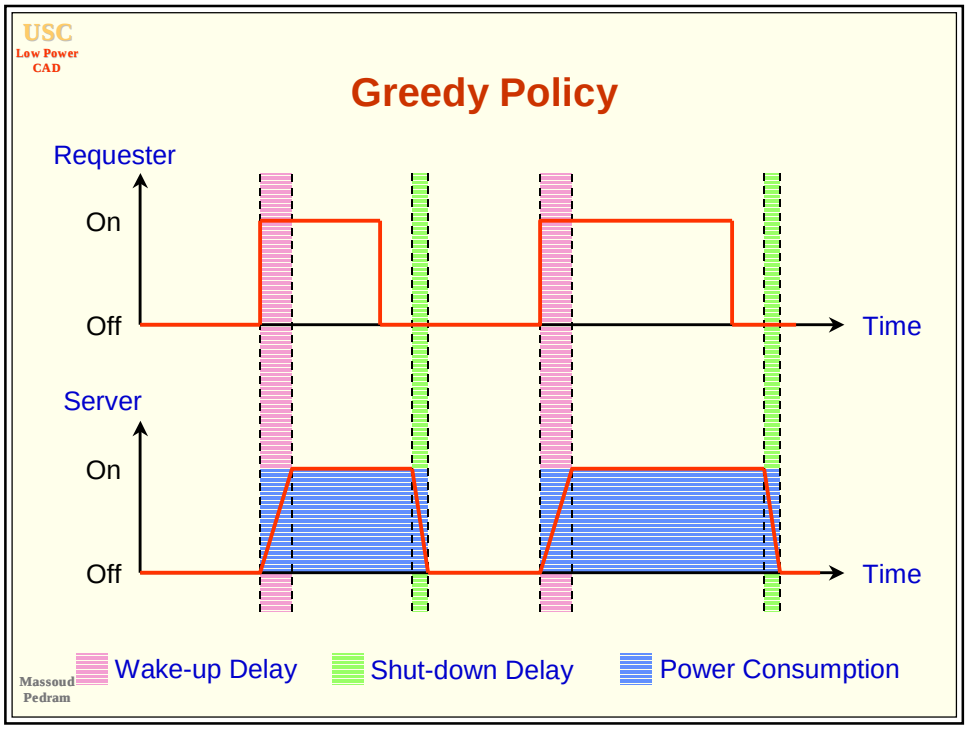
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CAD
Greedy Policy
Requester
On
Off
Time
Server
On
Off
Time
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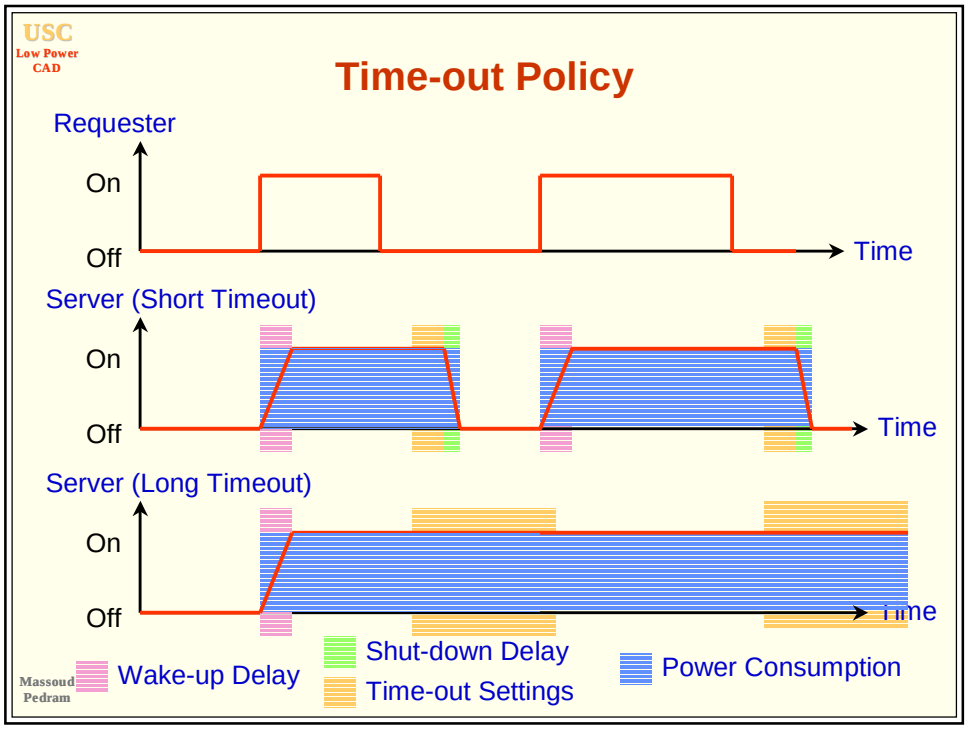
Wake-up Delay
Shut-down Delay
Power Consumption


USC
Low Power
CAD
Time-out Policy
Requester
On
Off
Time
Server (Short Timeout)
On
Off
Time
Server (Long Timeout)
On
Off
Time
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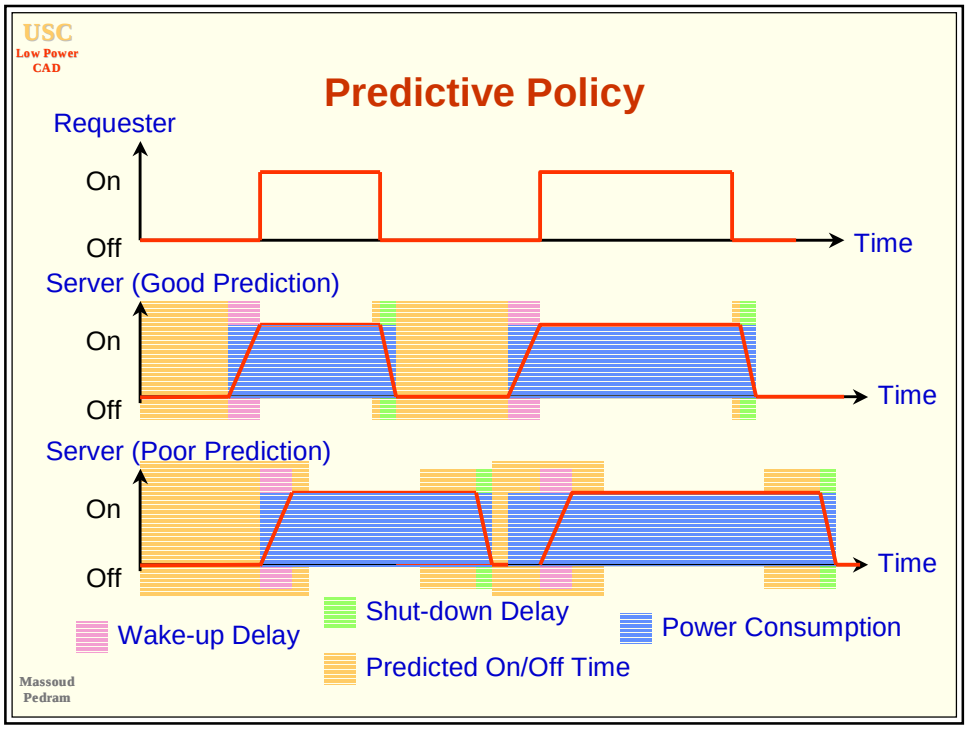
Wake-up Delay
Shut-down Delay
Time-out Settings
Power Consumption


USC
Low Power CAD
Predictive Policy
Requester
On
Off
Time
Server (Good Prediction)
On
Off
Time
Server (Poor Prediction)
On
Off
Time
Wake-up Delay
Shut-down Delay
Predicted On/Off Time
Power Consumption
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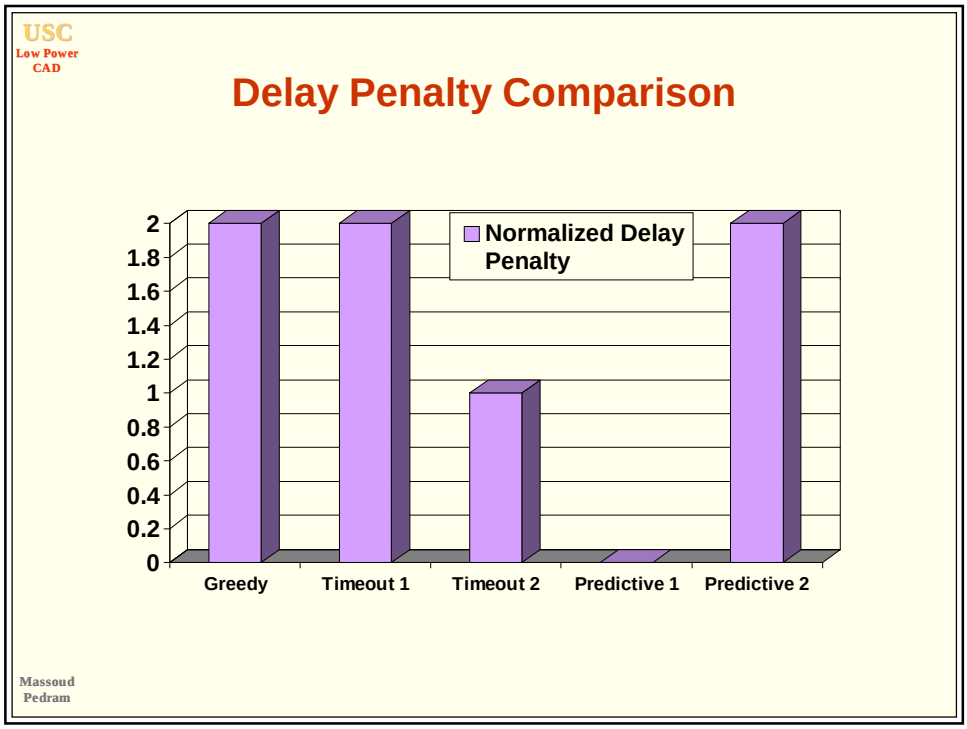
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Delay Penalty Comparison
Normalized Delay Penalty
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
Greedy
Timeout 1
Timeout 2
Predictive 1
Predictive 2
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Shortcomings of Previous Approaches

- Performance highly depends on workload characteristics
- No guarantee of optimality
- Cannot handle more than two power states
- Cannot handle complex systems

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Stochastic Approaches

- A generalized approach based on continuous-time Markov decision processes
- Adaptive and efficient
- Achieves optimal power under any given delay constraint (or vice versa)
- Can be extended to handle non-stationary data, multiple servers and requesters, correlations among system state transitions

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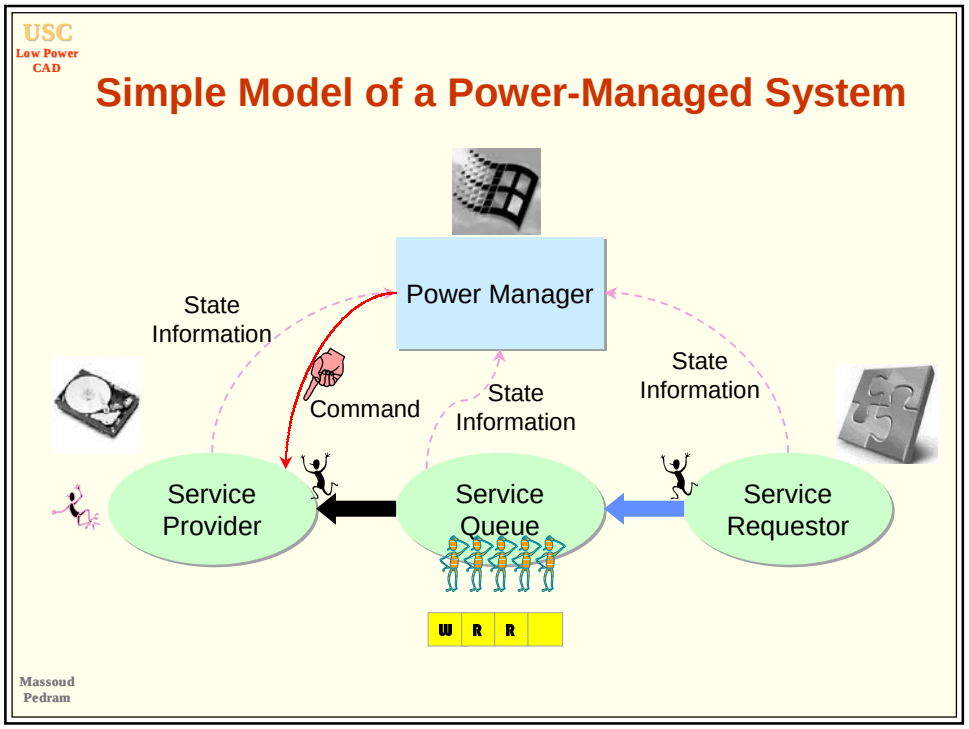
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Simple Model of a Power-Managed System
Power Manager
State Information
Command
State Information
State Information
Service Provider
Service Queue
Service Requestor
W R R
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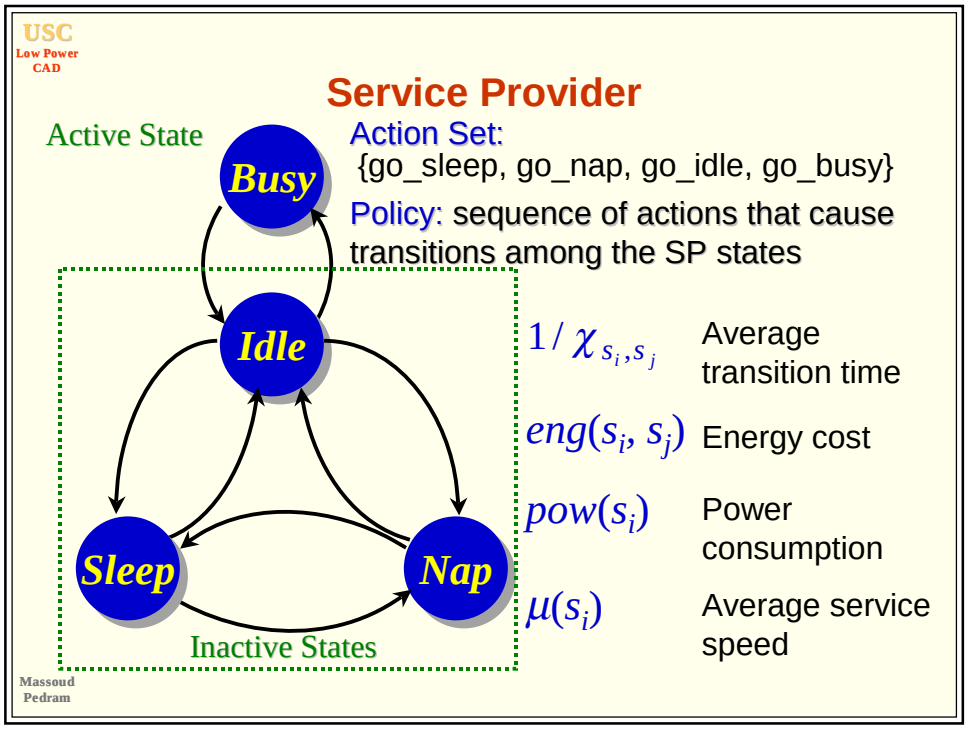
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Service Provider
Active State
Busy
Idle
Sleep
Nap
Inactive States
Action Set:
{go_sleep, go_nap, go_idle, go_busy}
Policy: sequence of actions that cause transitions among the SP states
$1/\chi_{s_i,s_j}$ Average transition time
$eng(s_i, s_j)$ Energy cost
$pow(s_i)$ Power consumption
$\mu(s_i)$ Average service speed
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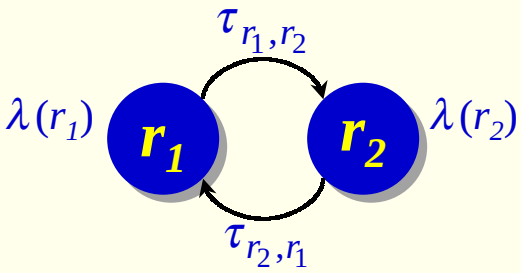
Service Requester



$\lambda(r_{1/2})$: Incoming rates for the requests

τ_{r_1,r_2} ,τ_{r_2,r_1} : State transition rates

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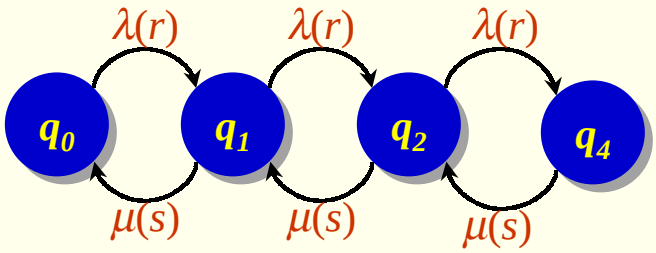
Service Queue (SQ)



$\lambda(r)$: Request incoming rate (depends on state *r* of the SR)

$\mu(s)$: Service rate (depends on state *s* of the SP)

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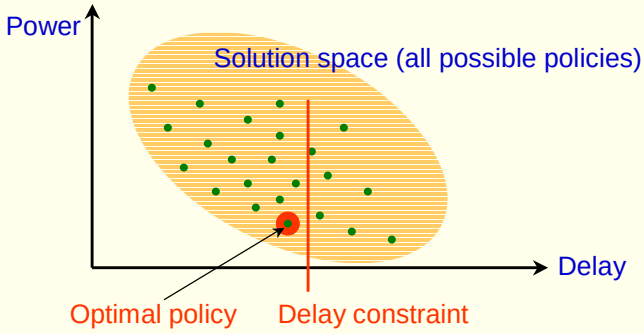
Problem Formulation

Find an optimal power management policy such that the system consumes minimum power while meeting a performance requirement



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Policy Optimization

- Linear Programming
  - ⇨ Optimal randomized policy (global optimal)
- Non-linear Programming
  - ⇨ Optimal deterministic policy
- Branch & Bound Algorithm
  - ⇨ Optimal deterministic policy
- Policy Iteration
  - ⇨ Heuristic only finds “convex” optimal policy
  - ⇨ Much faster than other algorithms

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Experimental Setup

- Model construction
  - SP model with four states
  - SR model with one state
  - SQ model of length 5
  - Exponential distribution of request inter-arrival times
- Comparison with other approaches
  - N-policy: Turn off the SP when the SQ is empty; Turn on the SP when there are N requests in the queue
  - Optimal when SP has two states

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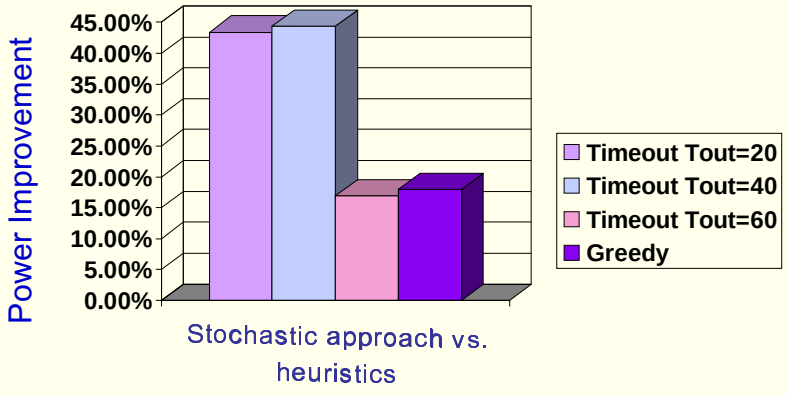
Power Savings 1



- In each case, we satisfy the constraint on average waiting time for requests

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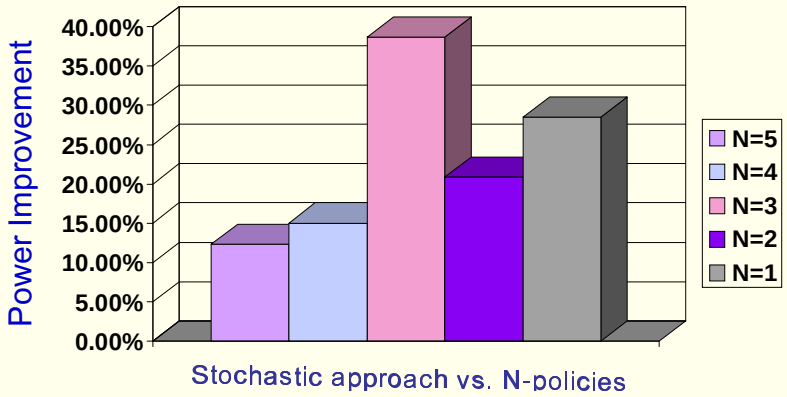
Power Savings 2



- In each case, we satisfy the delay constraints input requests

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Power-Aware C/C++ Compilers

- There exists a large amount of C/C++ code; rewriting them for low power is impractical. Instead we can recompile them for low power
- A power-aware compiler can help in choosing the best hardware architecture
- Compiler can insert commands into the application programs so that they can in turn provide detailed information to the OS for more effective power management

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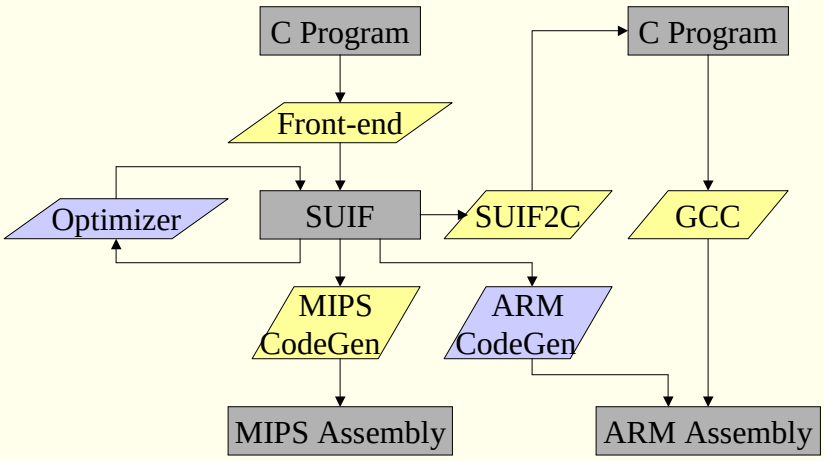
Example of a Compiler Flow



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Compiler-based Power Optimization

- **Reduce signal switching activities**
  - ⇨ **Prefer similar tags in cache (shorter Hamming distance)**
  - ⇨ **Replace expensive operations by inexpensive ones**
    - **0, 1, 4, 9, 16, 25…**
    - **F(I) = I * I**
    - **F(I+1) = F(I) + 2*I + 1**
  - ⇨ **Reorder instructions to reduce switching activity in control flow**
  - ⇨ **Select register number to reduce switching activity in data path**
- **Reduce cache misses**
  - ⇨ **Reorder aggregate data structure to improve spatial locality and reduce cache miss**

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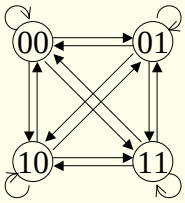
DRAM Address Bus Encoding

- Example:
  - ⇨ 4-bit address space, 2-bit bus
- Minimize switching activity on the 2-bit bus
- Modeled as an Eulerian Cycle Finding Problem
- Also works for the Burst Read mode



Eulerian		Gray		Binary	
value	b1b0	Value	b1b0	value	b1b0
0000	00 00	0000	00 00	0000	00 00
0001	00 01	0001	00 01	0001	00 01
0101	01 01	0011	00 11	0010	00 10
0100	01 00	0010	00 10	0011	00 11
0011	00 11	0110	01 10	0100	01 00
1111	11 11	0111	01 11	0101	01 01
1101	11 01	0101	01 01	0110	01 10
0111	01 11	0100	01 00	0111	01 11
1110	11 10	1100	11 00	1000	10 00
1001	10 01	1101	11 01	1001	10 01
0110	01 10	1111	11 11	1010	10 10
1010	10 10	1110	11 10	1011	10 11
1000	10 00	1010	10 10	1100	11 00
0010	00 10	1011	10 11	1101	11 01
1011	10 11	1001	10 01	1110	11 10
1100	11 00	1000	10 00	1111	11 11
	8+8 =16		16+16 =32		15+15 =30

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Conclusions

- Low power design is a critical area of research and development
- Need early power analysis and estimation to enable high level optimizations
- OS-directed power management and compiler-based power optimization hold the key to significant power reduction

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