Optimizing the Energy-Delay-Ringing Product in On-Chip CMOS Line Drivers

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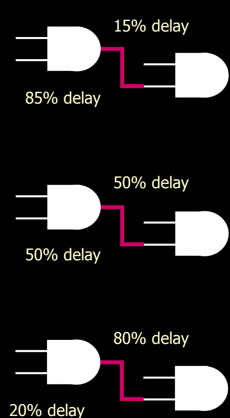
Outline

- Introduction
- Problem Statement
- Transmission Line Modeling
- Energy-Delay-Ringing Product(New Metric)
- Simulation Results
- Summary

Introduction

- System-level electrical issues are becoming more critical
  - Higher clock rates
    - wires are transmission lines
    - clock skew and jitter are a major portion of a clock cycle
  - Lower voltages
    - more current for a given power level
    - less margin
  - Pin bottlenecks
    - need to make each signal count

Wire Delay



- Mid 80 Scenario
  - Most of the input to output delay of the logic is due to gate delay
- Mid 90 Scenario
  - Half of the input to output delay of the logic is due to wire delay
- Today's Scenario
  - Most of the input to output delay of the logic is due to wire delay

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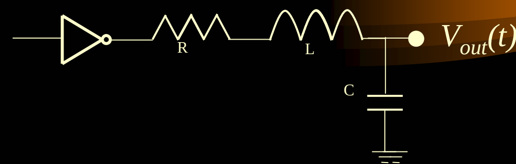
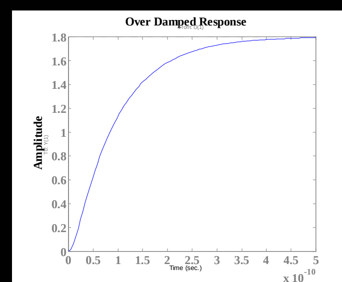
Problem Statement



Weak inductive effect



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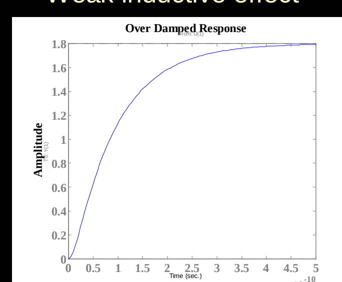
Problem Statement

Significant inductive effect

Weak inductive effect



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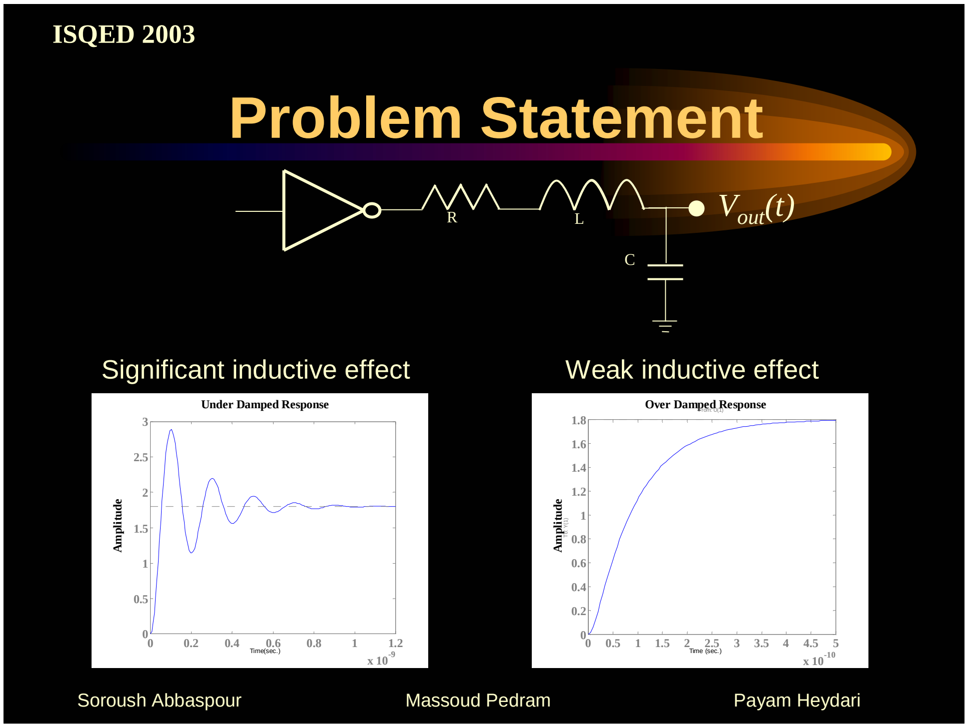
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Problem Statement
R
L
C
Vout(t)
Significant inductive effect
Weak inductive effect
Under Damped Response
Over Damped Response
Amplitude
Time(sec.)
x 10-9
Time (sec.)
x 10-10
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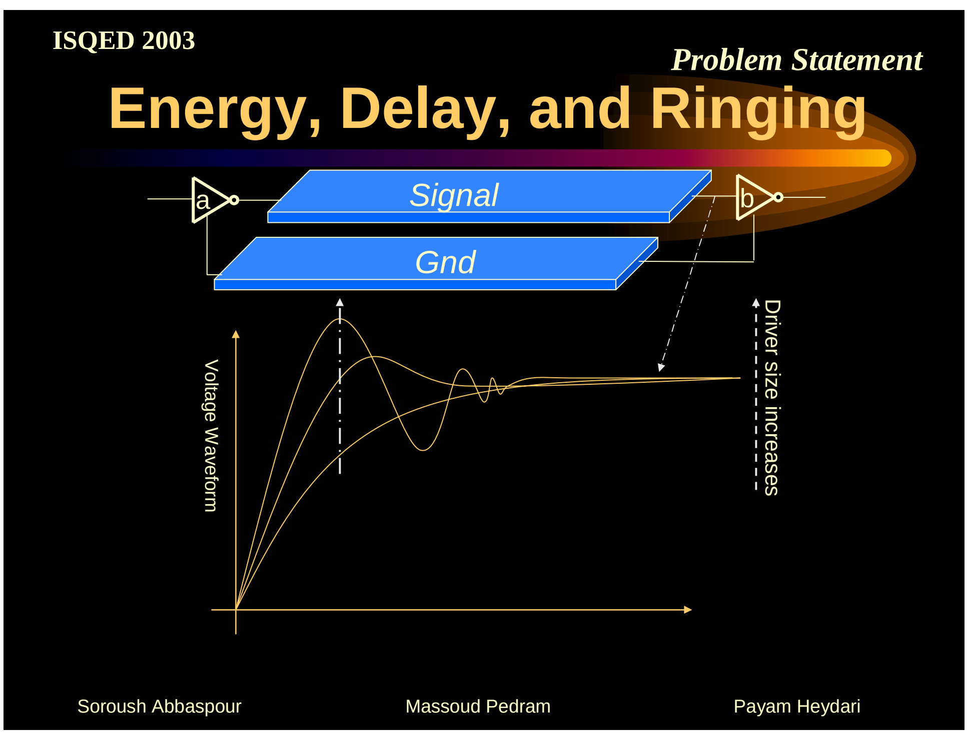
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Problem Statement
Energy, Delay, and Ringing
a
Signal
b
Gnd
Voltage Waveform
Driver size increases
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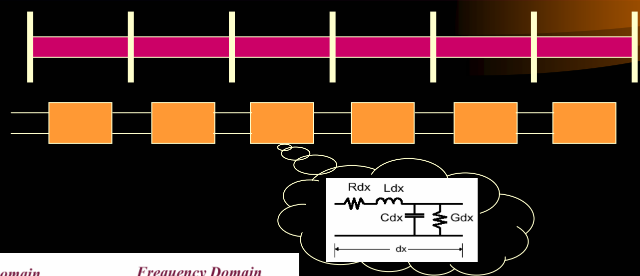
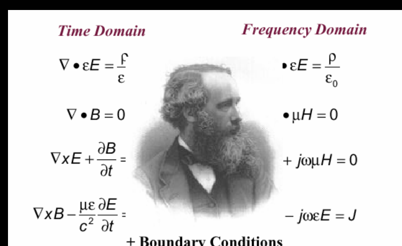
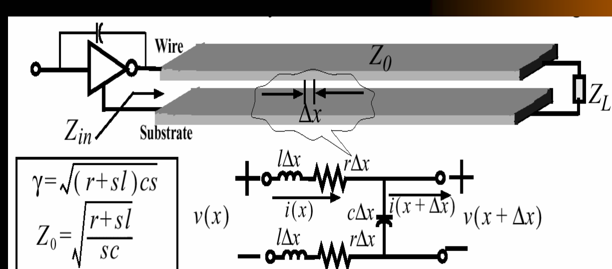
Transmission Line Theory





- We should think of Maxwell equations to analyze the transmission lines accurately.

Characteristics of the Line



$$Z_{in}\Big|_{x=-h} = Z_O \frac{Z_L + Z_O \tanh(\gamma h)}{Z_O + Z_L \tanh(\gamma h)}$$

$$H_v\Big|_{x=-h} = \frac{Z_L}{Z_o \cosh(\gamma h) + Z_L \sinh(\gamma h)}$$

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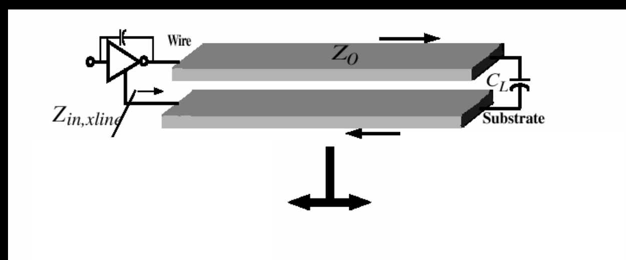
Transmission Line Theory

New Energy Model

- Need to efficiently model the energy dissipation of on-chip interconnect driven by CMOS drivers
  - Truncating the Zin(s) gives you a model for energy



(a) RLC equivalent circuit (b) RLC-π equivalent circuit

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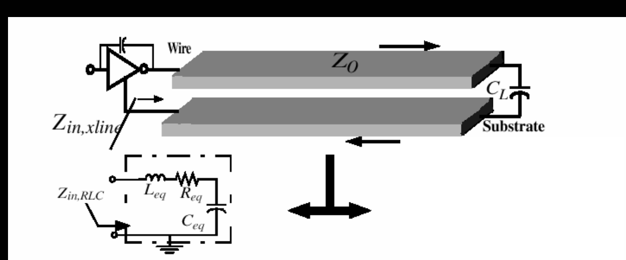
Transmission Line Theory

New Energy Model

- Need to efficiently model the energy dissipation of on-chip interconnect driven by CMOS drivers
  - Truncating the Zin(s) gives you a model for energy
    - First order truncation: *tanh(γh)*→*γh* gives RLC model



(a) RLC equivalent circuit (b) RLC-π equivalent circuit

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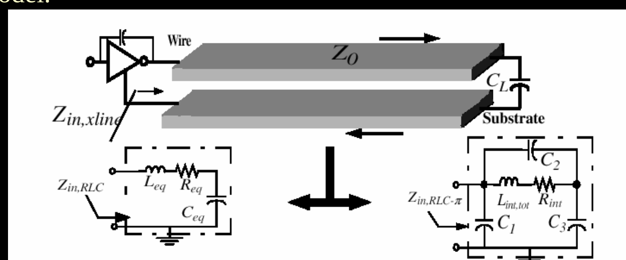
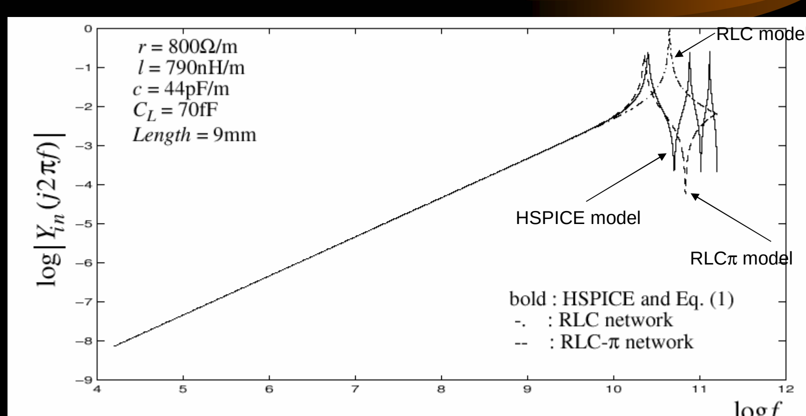
New Energy Model

- Need to efficiently model the energy dissipation of on-chip interconnect driven by CMOS drivers
  - Truncating the Zin(s) gives you a model for energy
    - First order truncation: $tanh(\gamma h) \rightarrow \gamma h$ gives RLC model
    - Second order truncation: $tanh(\gamma h) \rightarrow 2\gamma h/(2+\gamma^2 h^2)$ results in an RLC-π model.



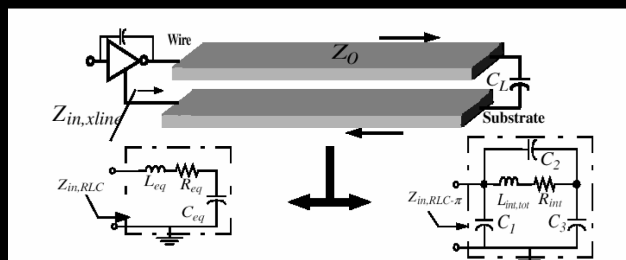
(a) RLC equivalent circuit (b) RLC-π equivalent circuit

RLC-π vs. RLC Energy Model



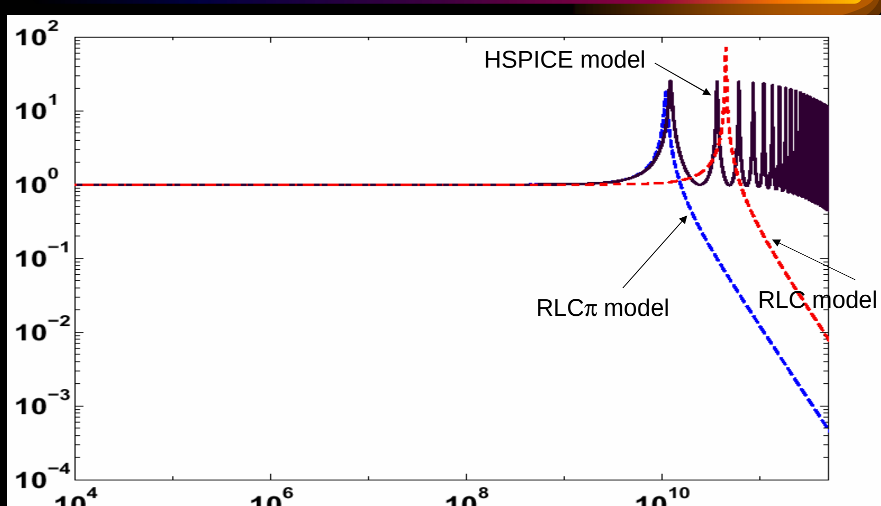
New Delay Model

- Need to efficiently model the delay of the on-chip interconnect
  - Truncating the H(s) results in a model for delay
  - The same scenario holds for delay with new values of R, L, C_1 C_2 and C_3.



(a) RLC equivalent circuit (b) RLC-π equivalent circuit

RLC vs. RLC-π Delay Model



RLC-π Energy and Delay Model

- Energy Parameters of Transmission Line

$$C_3^E = \sqrt{\frac{(C_{int,tot} + C_L)^2 + C_L^2}{2}} \quad , \quad C_2^E = \frac{C_{int,tot}}{2} + C_L - C_3^E$$

$$C_1^E = C_{int,tot} + C_L - C_3^E$$

- Delay Parameters of Transmission Line

$$C_1^D = \frac{C_{int,tot}}{2} \; , \quad C_2^D = 0 \; , \quad C_3^D = \frac{C_{int,tot}}{2} + C_L$$

$$L_{eq}^D = L_{int,tot} \; , \quad R_{eq}^D = R_{int,tot}$$

Energy-Delay-Ringing Product

- The wire length is determined by the routing constraints.
- Driver upsizing
  - will increase the energy dissipation
  - will decrease the 50% propagation delay
- Increasing the current drive capability of the line driver causes the inductive effects to become more important
  - Ringing will increase the settling time
- Change the driver size to achieve the best Energy-Delay-Ringing Product

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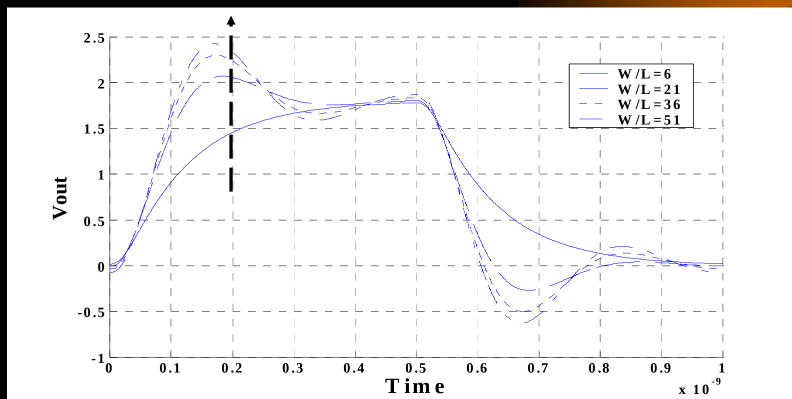
Energy-Delay-Ringing Product

Output Voltages for Different Driver Sizes



- V_{out} as a function of four different W/L driver values

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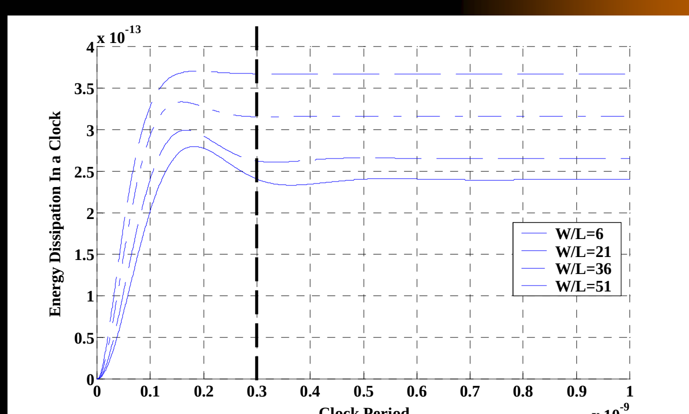
Energy-Delay-Ringing Product

Energy for Different Driver Sizes



- Energy dissipation in a clock cycle as a function of the clock period for four different driver *W/L* ratios

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Energy-Delay-Ringing Product

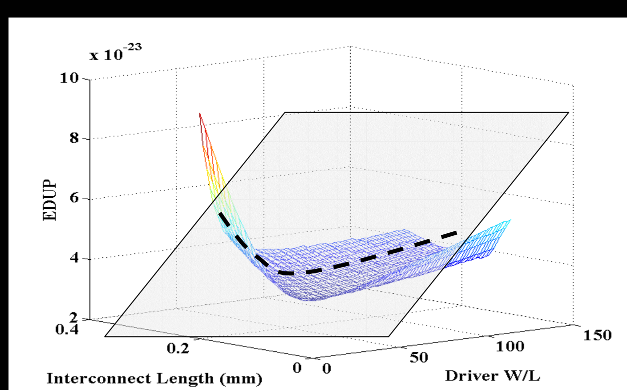
Why EDR-P

- Overdamped response ⟺ 50% delay is important
- Underdamped response ⟺ settling time is important
- Changing the driver size, varies the output waveform from overdamped to underdamped behavior.
- Propose a new metric; *Energy-Delay-Ringing Product*

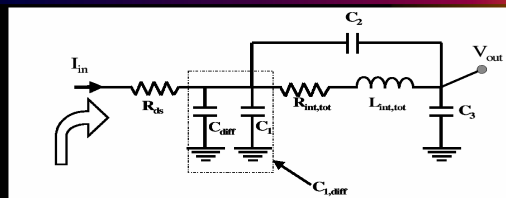
Energy-Delay-Ringing Product

EDR Product Diagram

The size of driver "b" is constant.



Energy and Delay Analysis



$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

where

$$a_2 = L_{int} C_2^E \qquad a_1 = R_{int} C_2^E \qquad a_0 = 1$$

$$b_3 = R_{ds} L_{int} (C_{1,diff}^E C_2^E + C_{1,diff}^E C_3^E + C_2^E C_3^E)$$

$$b_2 = L_{int}(C_2^E + C_3^E) + R_{ds} R_{int} (C_{1,diff}^E C_2^E + C_{1,diff}^E C_3^E + C_2^E C_3^E)$$

$$b_1 = R_{ds}(C_{1,diff}^E + C_3^E) + R_{int}(C_2^E + C_3^E) \qquad b_0 = 1$$

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Energy-Delay-Ringing Product

Approximation

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \Rightarrow \frac{V_{out}(s)}{V_{in}(s)} \cong \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0}$$

$$\frac{I_{in}(s)}{V_{in}(s)} = \frac{d_3 s^3 + d_2 s^2 + d_1 s}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} = 1 - \frac{L_{int}(C_2^E + C_3^E)s^2 + R_{int}(C_2^E + C_3^E)s + 1}{L_{int} C_2^E s^2 + R_{int} C_2^E s + 1} \times \frac{V_{out}(s)}{V_{in}(s))}$$

$$d_3 = L_{int}(C_{1,diff}^E C_2^E + C_{1,diff}^E C_3^E + C_2^E C_3^E)$$

$$d_2 = R_{int}(C_{1,diff}^E C_2^E + C_{1,diff}^E C_3^E + C_2^E C_3^E)$$

$$d_1 = C_{1,diff}^E + C_3^E$$

$$\Downarrow$$

$$\frac{I_{in}(s)}{V_{in}(s)} = \frac{d_2 s^2 + d_1 s}{b_2 s^2 + b_1 s + b_0}$$

The same scenario holds for delay analysis

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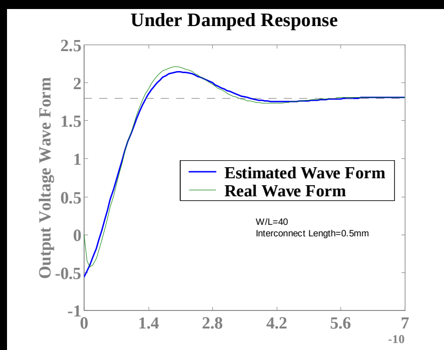
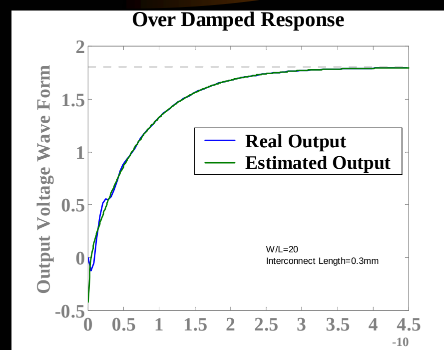
Simulation Results

Comparison for Two Different Responses





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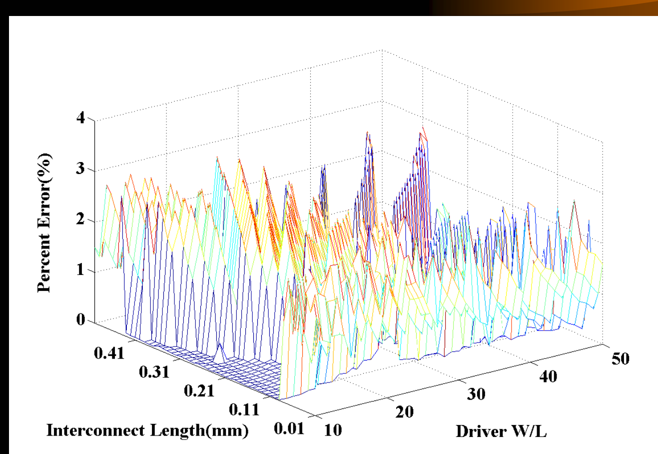
Simulation Results

Approximation Error



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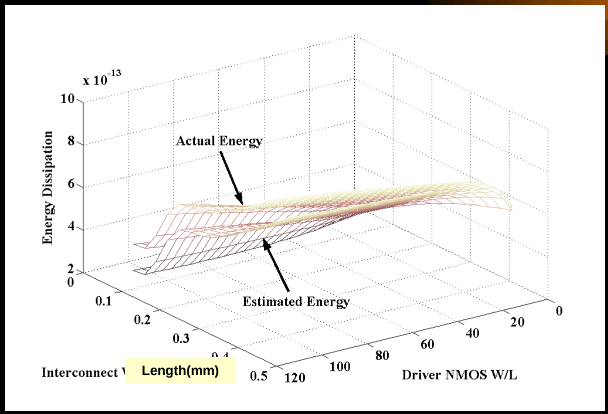
Simulation Results

Energy Dissipation: Simulation vs. Analytical Model



- Difference between simulation and analytical model for different interconnect lengths and driver sizes

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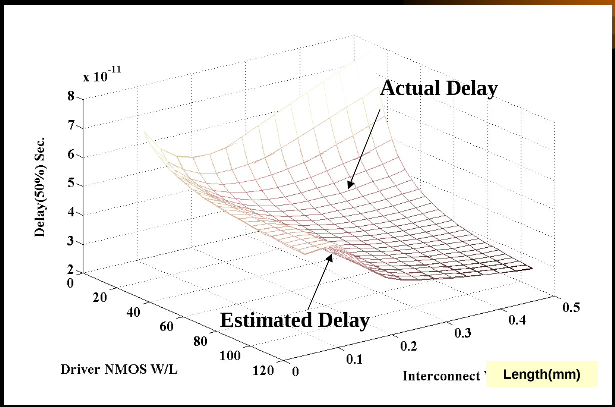
Simulation Results

Delay: Simulation vs. Analytical Model



- Difference between real Delay and estimated Delay in 0.18µm technology for different interconnect lengths and driver sizes

Summary

- We presented new transmission line energy and delay models for high frequencies
- We defined a new metric which is EDR-P
- We proposed closed form expressions for energy, delay and ringing.
- Simulation results verify the accuracy of the proposed analytical model.