

# A SYNTHESIS METHODOLOGY FOR ECL CIRCUITS BASED ON MIXED VOLTAGE-CURRENT REPRESENTATION\*

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**Abstract** This paper presents a synthesis methodology for ECL circuits based on a mixed voltage-current signal representation and operation defined on the voltage and current signals. The ideas presented in this paper are then demonstrated on the design of an ECL 1-bit full adder. The paper concludes by presenting an algebra system which is suitable for current signal representation and operation on currents.

**Key words** current signal; circuit synthesis; ECL; algebraic system

## I. Mixed Voltage-Current Representations in ECL Circuits

In the traditional design of digital circuits, voltage is generally used to represent the logic signal. For example, if the positive logic convention is used, two values of a variable, 1 and 0, are represented by two voltage levels, high and low. (For negative logic convention, the values are inverted.) However, signals in ECL circuits are represented by both voltage and current.<sup>[1]</sup> Consider the ECL restorer/inverter shown in Fig.1(a) as an example. In this circuit the reference voltage (-1.2V), which is labeled by 0.5, is set in the middle of the high level (-0.8V) and low level (-1.6V). Assuming an input voltage signal  $V_x = -0.8V$  (high level), the unit current  $I_0$  will pass through the input transistor while no current (0) passes through the reference transistor. Consequently, current signals flow through the collector resistor  $R_0$  and are transformed into the corresponding voltage signals. If  $(I_0R_0)$  equals the unit voltage 0.8V, the two voltage signals at nodes  $P$  and  $Q$  will be -0.8V and 0V, respectively. Because of the voltage drop across the b-e junctions of two output emitter followers (output load resistors are not shown in this paper), the output signal will be level-shifted down by 0.8V. Thus, we have  $V_{re} = -0.8V$  and  $V_{\bar{x}} = -1.6V$ . If the input voltage signal  $V_x = -1.6V$  (low level), the discussion will be similar. It is seen that current signal is another signal form in ECL circuits. Thus, by introducing operations applicable to current signals, we may have a mixed methodology to synthesize ECL circuits.

In the above discussion we also notice that if the current signal ( $I_0, 0$ ) corresponds to logic value (1, 0), the output voltage signal (-1.6V, -0.8V), which is first transformed from the current signal and then level shifted by the emitter-follower, should be (1, 0), too. Therefore, the voltage signal in ECL circuits should take the negative logic convention in nature. We adopt the negative logic convention in this paper. Thus, the circuits shown in Figs.1(b) and 1(c) are renamed AND/NAND gate and OR/NOR gate rather than their traditional names, which are based on positive logic convention. For example, voltage relationship and the corresponding truth table with negative logic convention at node  $P$  in Fig.1(b) are shown in Fig.1(d). The NAND operation, rather than NOR operation, is given in the truth table.

## II. Physical Operations on Voltage Signals and Current Signals

The characteristics of voltage signals are such that they can be easily compared with one another. Taking the bipolar transistor as the example, the forward characteristics of a p-n junction can be used to compare and select voltage signals, as shown in Fig.2 (we omit here the voltage drop across all pn junctions).<sup>[2]</sup> It is clear that with negative logic convention circuits in Figs.2(a),2(b),2(c) execute the OR operation whereas circuits in Figs.2(d),2(e),2(f) execute the AND operation. (With positive logic convention, the two operations are exchanged.) In ECL

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circuits, the configuration in Fig.2(f) is used to realize AND operation among inputs, as shown in Fig.1(b). The wired AND operation could also be realized by tying the emitter outputs of two transistors.

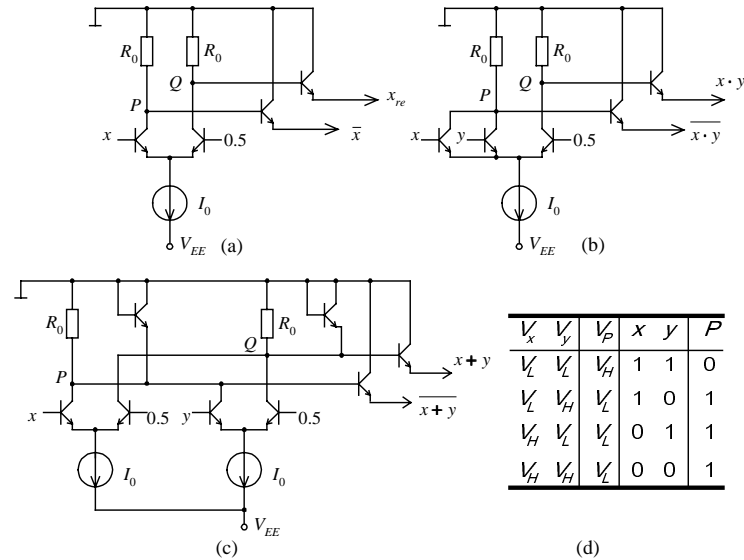


Fig. 1. Basic ECL gates

(a) restorer/inverter, (b) AND/NAND gate (negative basic convention), (c) OR/NOR gate (negative logic convention), (d) truth table for node  $P$  in AND/NAND gate (negative logic convention)

The situation is different for the current signals since they are difficult to compare with one another. We can now understand why current signals are seldom discussed in the traditional design using Boolean operations. However, current signals are easy to add or subtract by simply tying wires with each other. This indicates that if addition and subtraction are introduced as the auxiliary operations, the synthesis technique for ECL circuits will be enhanced. In the circuit of Fig.1(c), we find that when  $V_x = V_y = -0.8V$ , both input transistors in two transistor-pairs are conducting and there will be an added current of  $2I_0$  flowing through the node  $P$ . This reflects a realistic addition operation in an ECL circuit. However, current  $2I_0$  would generate logic value 2, thus the addition operation may lead to a high logic value, which is outside the allowed logic range (1, 0). The standard answer is to truncate it to avoid the appearance of a high logic value. In Fig.1(c) a clipping diode is connected in parallel with the resistor  $R_0$  to truncate the voltage excess. (Note that the current excess would generate a voltage excess in the absence of the clipping diode.) Its action can be also explained by a minimum comparison operation in Fig.2(d). In fact, the OR operation in Fig.1(c) is realized by the following formula:

$$x + y = \min(x \& y, 1).$$

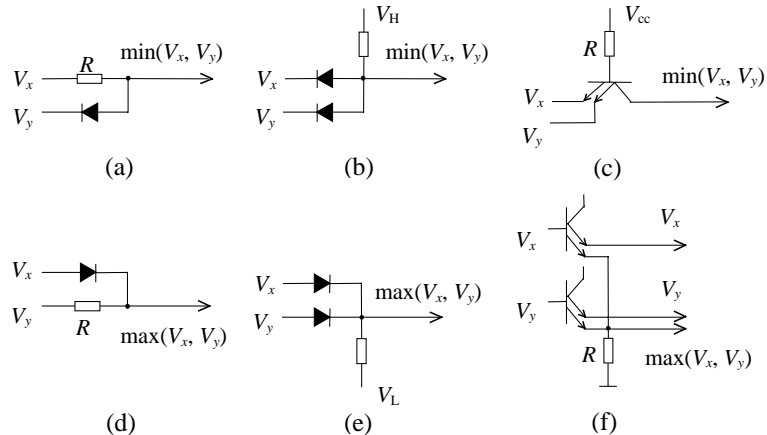


Fig.2 Comparison of voltage signals by p-n junction and Boolean operations

### III. Design of ECL Circuits by Using Excess-Valued Current Signals

In the preceding section we described how to restrain the signal to avoid the excess-valued logic level. However, the excess-valued level can significantly increase the amount of information carried in wires and the information processed by transistors. It is thus expected that using excess-valued signal will lead to a less complex circuit construction. In this section we will take into account the excess-valued signal generated by addition operation of current signals. The excess-valued signal can act on the reference side as well as the signal side of the differential transistor-pair. We will apply the proposed synthesis technique to the design of an ECL full adder.

A traditional design of an ECL full adder is shown in Fig.3, where the simplest construction is achieved by using “series-gates” connection.<sup>[3]</sup> Compared to the design which is composed of individual ECL gates to form the full adder, design of Fig.3 has the advantage of less complex construction, fewer cascade levels, and fewer current sources. It should be noted that to prevent transistors in lower levels from saturation, the input signals and references have to be level-shifted down. For the second level, the voltages corresponding to  $B'(1,0)$  are  $(-2.4V, -3.2V)$ , and the reference  $0.5'$  corresponds  $-2.8V$ . This means that both the input signal and reference are level-shifted down by  $1.6V$ . For the lowest level, the input signal  $A''$  and the reference  $0.5''$  are level-shifted down by  $3.2V$ .<sup>[4]</sup> In Fig.3 we find that node  $P$  (or  $Q$ ) is connected to only one current source  $I_0$  in any case, thus the “added” current at node  $P$  (or  $Q$ ) would never be an excess-valued signal.

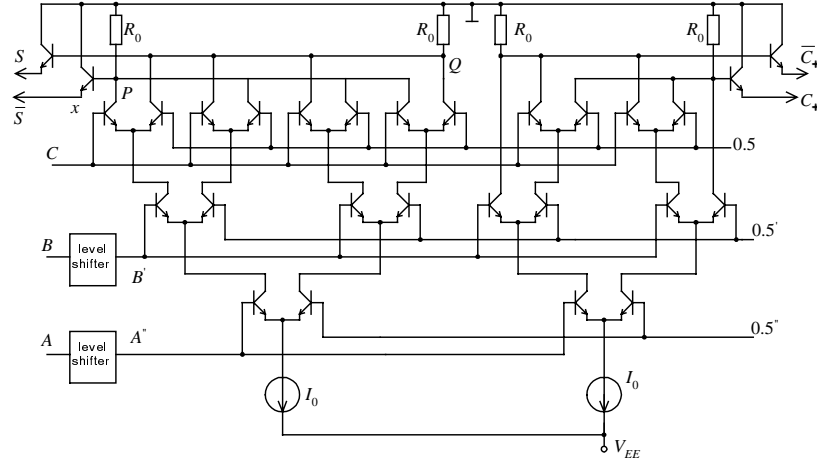


Fig.3. Traditional design of ECL full adder with series-gates

It is natural that the addition of  $A$ ,  $B$ , and  $C$  leads to a four-valued sum signal,  $\Sigma=0,1,2,3$ . The sum signal can be easily realized by current signal, as shown in Fig.4(a), where the transformed voltage signal at node  $P$  is also a four-valued signal  $(0, -0.8V, -1.6V, -2.4V)$  corresponding to the four-valued current signal  $(0, I_0, 2I_0, 3I_0)$ .<sup>[5]</sup> In order to prevent the transistors from saturation, the input signals  $A$ ,  $B$ ,  $C$  and the reference  $0.5'$  should be level-shifted down by  $1.6V$ . Four levels of the output sum signal  $\Sigma$  in Fig.4(a) are  $(-0.8V, -1.6V, -2.4V, -3.2V)$  due to the b-e junction of the emitter follower. Similarly, we can derive its complementary signal  $\bar{\Sigma}$ . Its corresponding four output levels are  $(-3.2V, -2.4V, -1.6V, -0.8V)$ . If the level-shifted sum signal  $\Sigma'$   $(-1.6V, -2.4V, -3.2V, -3.6V)$  and the reference  $0.5'$   $(-2.8V)$  are applied to two sides of a transistor-pair, the carry-out signal  $C_+$  will be obtained, as shown in Fig.4(b). In this circuit we also generate a signal  $\bar{C}_+$ . Corresponding to four levels  $(-0.8V, -1.6V, -2.4V, -3.2V)$  of  $\Sigma$ , the output levels are  $(-2.8V, -2.8V, -1.2V, -1.2V)$  of  $\bar{C}_+$  since the collector resistor is  $2R_0$  and there is a bias current source  $0.25I_0$ . Obviously, if the signal  $\bar{C}_+$  is

taken as a variable reference, and the complementary sum signal  $\bar{\Sigma}$  is the input, we will get the sum signal  $S$  and its complement  $\bar{S}$ , as shown in Fig.4(c).

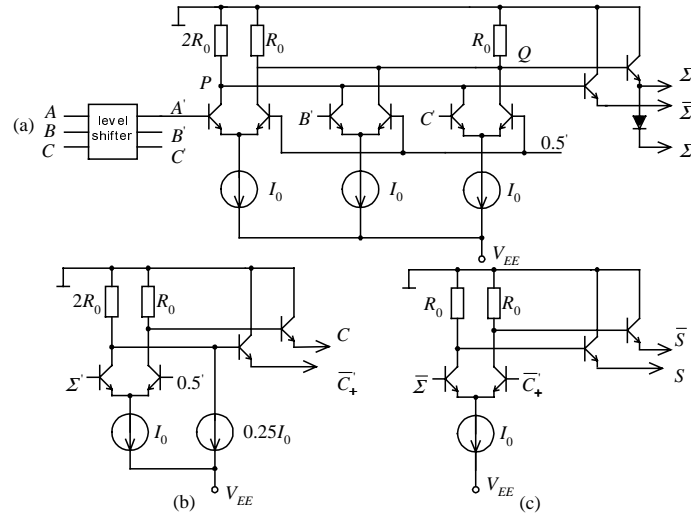


Fig.4. Design of ECL full adder by using excess-valued addition signals

Comparing the two designs in Fig.3 and Fig.4, we find that the design in Fig.4 is much smaller. In the whole design only five transistor-pairs are needed instead of twelve pairs in Fig.3. In addition, in the design only one reference voltage level is needed (compared to three in Fig.3). However, it has more current source and cascade level. The circuit in Fig.4 has proved to have ideal logic function by PSPICE simulation, as shown in Fig.5. It should be pointed out that the intermediate excess signal  $\Sigma$  can be used to realize other symmetric functions  $f_S(A,B,C)$  with a simple structure, thereby, the circuit in Fig.4(a) to generate  $\Sigma$  is useful in other design.

#### IV. An Algebra System Suitable for Current Signals

For any new operation, the proper position in an algebra system, as well as its corresponding physical realization in the circuit should be clear. We therefore need to establish a corresponding algebra system suitable for current signals by referencing to the Boolean algebra which is suitable to voltage signals.

As indicated in Section II, the traditional Boolean operations are relative to comparison. Three basic operations, AND, OR and NOT, can be re-defined by comparison operation as below.<sup>[2]</sup>

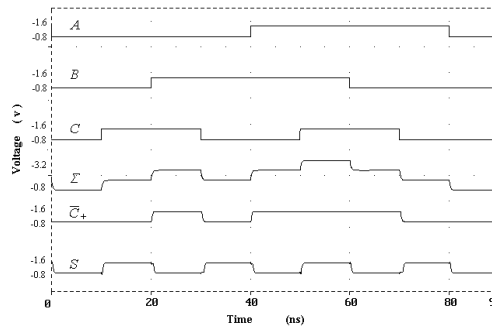


Fig.5. SPICE simulation of the ECL full adder by using excess-valued addition signals

AND (minimum operation)

$$x \cdot y = \min(x, y), \quad (1)$$

OR (maximum operation)

$$x + y = \max(x, y), \quad (2)$$

NOT (threshold comparison)

$$\bar{x} = \begin{cases} 0, & \text{if } x > 0.5; \\ 1, & \text{if } x < 0.5. \end{cases} \quad (3)$$

It is well known that AND, OR and NOT form a complete set to express arbitrary functions. For example, a two-input function  $f(x,y)$  shown in Tab 1, where  $c_i \in \{0,1\}$ , can be expressed by the following canonical minterm expansion form:

$$f(x, y) = c_0 \cdot (\bar{x} \cdot \bar{y}) + c_1 \cdot (\bar{x} \cdot y) + c_2 \cdot (x \cdot \bar{y}) + c_3 \cdot (x \cdot y). \quad (4)$$

**Tab 1** 2-input logic function

$x$	$y$	$f(x,y)$
0	0	$c_0$
0	1	$c_1$
1	0	$c_2$
1	1	$c_3$

Actually, the above equation describes the procedure to look up Tab.1 by using a type of algebraic language. For instance, the first term  $c_0 \cdot (\bar{x} \cdot \bar{y})$  in Eq.(4) shows that when  $x = 0$  and  $y = 0$  the function value is checked out as  $c_0$ , and so forth.

Since the voltage signal are easy to compare with each other, Boolean algebra based on comparison lattice is suitable to circuit design with voltage signal representation. However, if current signal representation is used, the arithmetic operation, such as addition and subtraction, can be easy to realize by simply tying wires. By restraining signal being binary, we may introduce the following bounded arithmetic operations to avoid cases of  $1 \& 1 = 2$  and  $0 - 1 = -1$ .

*Bounded addition*

$$x \uplus y = \min(1, x \& y) = \begin{cases} 1, & \text{if } x \& y > 1; \\ x \& y, & \text{otherwise.} \end{cases} \quad (5)$$

*Bounded subtraction*

$$x \ominus y = \max(0, x - y) = \begin{cases} 0, & \text{if } x - y < 0; \\ x - y, & \text{otherwise.} \end{cases} \quad (6)$$

We can prove that these two bounded operations may be expressed with traditional Boolean operation, AND, OR and NOT, as follows:

$$x \uplus y = x + y, \quad (7)$$

$$x \ominus y = x \cdot \bar{y}. \quad (8)$$

If  $x = 1$  in Eq.(8), we can obtain NOT operation:

$$1 \ominus y = \bar{y}. \quad (9)$$

Since OR and NOT form a complete set, the above two bounded operation also form a complete set. By using bounded operations we can express the two-input function in Tab.1 with the following canonical expansion:

$$f(x, y) = [c_0 \Theta(x \uplus y)] \uplus [c_1 \Theta(x \uplus \bar{y})] \uplus [c_2 \Theta(\bar{x} \uplus y)] \uplus [c_3 \Theta(\bar{x} \uplus \bar{y})]. \quad (10)$$

The above equation also describes the procedure to look up Tab.1 by using another algebraic language. For instance, when  $x = 0$  and  $y = 0$  only the term  $(x \uplus y)$  is 0 and only the first term  $c_0 \Theta(x \uplus y)$  in Eq.(10) remained so that the function value is checked out as  $c_0$ , and so forth. Eq.(10) is specifically used for current-mode circuits, where all signals are represented by current. However, in ECL circuits we usually need mixed voltage-current operations in circuit synthesis. As an example, if  $c_0 = 1$  and  $c_1 = c_2 = c_3 = 0$  in Eq.(10), we have

$$f(x, y) = 1 - (x \uplus y) = \overline{\min(x \& y, 1)},$$

where operation  $x \& y$  is realized with current signals and minimum operation is realized with voltage signal. This shows that there does exist another algebra system for current signals and it offers a theoretic basis for using current signal. However, it is particularly suitable for pure current-mode circuits, such as current-mode CMOS circuits.<sup>[6]</sup>

Finally, we should indicate that by using Eqs.(7) and (8), Eq.(10) returns to Eq.(4):

$$f(x, y) = [c_0 \cdot \overline{x + y}] + [c_1 \cdot \overline{x + \bar{y}}] + [c_2 \cdot \overline{\bar{x} + y}] + [c_3 \cdot \overline{\bar{x} + \bar{y}}].$$

The above discussion shows that the current signal representation has not only a physical basis but also an algebraic basis. The derived algebra system can be used to design current-mode circuits. However, since the voltage signal is dominant signal form in ECL circuits, Boolean algebra still plays a major role in designing ECL circuits. We believe that with the mixed current-voltage representation, specifically by using the intermediate excess-valued signal, a more flexible and powerful synthesis methodology for ECL circuits can be developed.<sup>[7]</sup>

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