# Semi-Analytical Current Source Modeling of FinFET Devices Operating in Near/Sub-Threshold Regime with Independent Gate Control and Considering Process Variation

Tiansong Cui, Yanzhi Wang, Xue Lin, Shahin Nazarian, and Massoud Pedram
Department of Electrical Engineering
University of Southern California
Los Angeles, California, United States, 90089
{tcui, yanzhiwa, xuelin, shahin, pedram}@usc.edu

***Abstract*—Operating circuits in near/sub-threshold region has shown effectiveness in lowering the energy consumption of digital circuits, but it can lead to a higher sensitivity to transient noise and also varies sources of variability. FinFET has been proposed as an alternative for bulk CMOS devices due to its more effective channel control, reduced random dopant fluctuation, high ON/OFF current ratio, lower energy consumption, etc. The characteristics of FinFETs operating in the near/sub-threshold region make it difficult to verify the timing of a circuit using conventional statistical static timing analysis (SSTA) method.**

**The current source modeling (CSM) technique has been applied to bulk CMOS circuits to increase the accuracy of timing analysis in dealing with arbitrary shapes of the input signal waveforms. This paper extends the CSM to FinFET devices operating in the near/sub-threshold voltage regime with independent gate control and subject to process variations. More precisely, we combine non-linear analytical models and low-dimensional CSM lookup tables to simultaneously achieve high modeling accuracy and time/space efficiency.**

## I. INTRODUCTION

Power efficiency has gained growing attention in VLSI design with the increasing demand for extending the battery life of portable devices as well as lowering the electrical energy cost of high-performance computing nodes. Aggressive voltage scaling from the traditional super-threshold region to the near/sub-threshold region has shown effectiveness in reducing the power consumption of digital circuits [1][2][3]. It is especially beneficial for applications with relaxed performance requirements, such as wireless sensor processing and medical monitoring, because the operating frequency of near/sub-threshold logic is much lower than that of traditional strong-inversion circuits ($V_{DD} > V_{th}$) due to the smaller transistor ON-current in the near/sub-threshold region. For example, according to [2], voltage scaling from super-threshold regime (e.g., 1.1V) down to the near-threshold regime (e.g., 0.5V) yields an energy reduction on the order of 10X at the expense of approximately 10X performance degradation.

With the dramatic downscaling of layout geometries, the traditional bulk CMOS technology is facing significant challenges due to several reasons such as the increasing leakage and short-channel effects (SCEs) [4]. FinFET devices, a special kind of quasi-planar double gate (DG) devices, have been proposed as an alternative for the bulk CMOS when technology scales beyond the 32nm technology node [5][6]. It has been proved in [22] that FinFET devices outperform bulk CMOS devices in ultra-low power designs by allowing for higher voltage scalability. Another unique feature of FinFET devices is the *independent gate control*, i.e., the front gate and the back gate can be controlled by separate signals, which enables more flexible circuit designs [8]. Due to the capacitor coupling of the front gate and the back gate, the threshold voltage of the front-gate-controlled FET varies in response to the back gate biasing, and vice versa. Previous work [7] utilized the independent gate control for FinFETs in the pull-down network of an SRAM cell to keep the ~20 pA/μm standby power budget, whereas the authors of [8][9] studied joint gate sizing and negative biasing on the back gate of FinFET devices and demonstrated significant power reduction.

Our main goal in this work is to design an accurate delay model that accounts for variability while considering the afore-mentioned features of FinFET devices. *Statistical static timing analysis* (SSTA) is a well-known method to verify the circuit timing subject various sources of variation and considerable efforts have been invested in developing voltage-based statistical gate delay models [11]. However, their accuracy is limited as the input and output voltage dependencies are approximated with input slew and output load. This would be more severe for FinFET devices working in the near/sub-threshold regime as crosstalk noise more severely impacts the signal integrity [10]for such devices [10]. Also process variation is typically handled by applying a first-order correction to the quantities of interest using the variations of the process parameter [11]. Due to the exponential relationship between transistor's ON-current and threshold voltage for FinFET devices operating in the near/sub-threshold regime, process variations of important parameters such as the effective gate length $L_{eff}$ and their impacts should be more carefully taken into account.

*Current source-based logic cell modeling* (CSM) has been introduced as an alternative approach for timing calculation and verification [12]~[16] in order to address key shortcomings of conventional voltage-based timing analysis methods. Instead of recording the delays and output slews in LUTs, the CSM method builds an equivalent circuit model for each logic gate using independent current sources and several equivalent capacitances. The values of current sources and capacitances are pre-characterized and recorded in *standard CSM LUTs*, where the terminal voltages are used as the index keys. The output waveforms are calculated in a discrete-time manner using pre-characterized LUTs based on given input waveforms. In presence of the input noise, the CSM method achieves very high accuracy in producing output waveforms and calculating delays, because the current and capacitances at various combinations of input and output voltages are all pre-characterized. In addition, the CSM method is much faster compared to a circuit simulator such as SPICE because the former indexes pre-characterized LUTs to obtain values of currents and capacitances. Finally, the LUT-based approach in CSM can be easily applied to different supply voltage regimes, and thus is very suitable for simulating and analyzing circuits that support burst-mode applications and operate in multiple supply voltage regimes. Thanks to these capabilities, CSMs are used in timing analysis and can effectively reduce errors in delay calculation.

To extend the CSM-based method to FinFET devices operating in the sub/near-threshold voltage regime, there are two key requirements as follows: (i) The model should appropriately capture the variations of the component values in the equivalent circuit model due to the variations of process parameters; (ii) It should account for the fact that the threshold voltage of the front-gate-controlled FET is affected by the back-gate voltage, and vice versa. In this work, two major sources of process variations are considered: *Line-Edge Roughness* (LER), which causes variations of the effective channel length, denoted by $\Delta L$, and *Gate Work-Function Variation* (WFV), which causes variations of the

intrinsic threshold voltage, denoted by $\Delta V_{th0}$ [19]. Considering these effects, the CSM method utilizes a general equivalent circuit model for FinFET devices. We need to determine all the driving current and equivalent capacitance values in this equivalent model given the applied voltages on the front-gate-controlled and back-gate-controlled fins, the output voltage, as well as process variation parameters $\Delta L$ and $\Delta V_{th0}$ for N-type and P-type FETs.

In order to reduce the memory storage requirements, previous work such as [14] and [16] store the LUTs for CMOS logic cells in the superthreshold regime under the nominal process conditions, and apply polynomial corrections for process variations. However, for FinFET devices operating in the sub/near-threshold regime, the relationship between the driving current and the gate voltages (and the threshold voltage) becomes exponential. Hence, the polynomial correction method is not sufficient to capture the effects of the back-gate (and front-gate) voltage and process variations for FinFET devices operating in the sub/near-threshold regime.

In this paper, we develop a semi-analytical approach for FinFET CSM operating in the sub/near-threshold regime, accounting for the unit feature of independent gate control as well as process variations. The proposed technique determines all the component values in this equivalent circuit model given the applied voltages on the front-gate-controlled and back-gate-controlled fins, the output voltage, as well as process variation parameters $\Delta L$ and $\Delta V_{th0}$ for N-type and P-type FETs. We use a simple example to illustrate the meaning of the term "semi-analytical". For one component value of interest, e.g., driving current $I$, we derive an analytical equation relating it to the terminal voltages $x$ and $y$, and variations $\Delta u$ and $\Delta v$ in process parameters. The functional form of this equation is the same for all combinations of terminal voltages and process parameters. However, the equation also depends on a set of pre-characterized regression coefficients stored in LUTs. Suppose $I(x,y,\Delta u,\Delta v) = \mathbf{A}(x,y)\cdot g\left(\frac{x}{\mathbf{B}(x,y)}, y, \Delta u\right)\cdot h\left(y, \frac{\mathbf{C}(x,y)}{\Delta v}\right)$, and coefficients $\mathbf{A}(x,y)$, $\mathbf{B}(x,y)$, and $\mathbf{C}(x,y)$ are stored in LUTs corresponding to the $(x,y)$ pair. The effect of $(\Delta u, \Delta v)$ on $I$ has been captured by the function itself. This example captures the basic principle of the semi-analytical approach although the actual FinFET CSM is much more sophisticated. Notice that we only use 2D LUTs in our semi-analytical method to reduce the storage space requirement. Although the characterization process is extensive, it is done only once and the results are stored into compact low-dimensional LUTs.

## II. Characteristics of FinFET Devices in Near/Sub-Threshold Regime

### A. Independent Gate Control for FinFET Devices

FinFET devices show better suppression of the short channel effect, lower energy consumption, higher supply voltage scaling capability, and higher ON/OFF current ratio compared with the bulk CMOS counterparts [6][7]. In addition to better control over the channel by using double gates, the FinFET structure allows for fabrication of separate front and back gates. In this structure, each fin is essentially the parallel connection of the *front-gate-controlled FET* and the *back-gate-controlled FET*, both with width $H$ equal to the height of the fin. A unique feature of FinFET devices is the *independent gate control*, where the front and back gates are tied to different control signals.

Independent gate control makes it possible to apply different voltages to the front and back gates of a single fin, and thereby, allowing for more flexible circuit designs. Due to capacitor coupling of the front gate and the back gate of a FinFET transistor, the threshold voltage of the front-gate-controlled FET varies in response to the back-gate voltage, and vice versa. Under a relatively small back-gate voltage, a linear relationship between the change of the threshold voltage and the back-gate voltage is observed (suppose we consider N-type FETs):

$$\frac{dV_{th}}{dV_{BN}} = -\frac{C_{oxb}\cdot C_{si}}{C_{oxf}\cdot(C_{oxb}+C_{si})} \qquad (1)$$

where $C_{si}$, $C_{oxf}$, and $C_{oxb}$ are the body capacitance, front-gate capacitance, and back-gate capacitance, respectively; $V_{BN}$ is the voltage level applied to the back gate of the N-type fin. Eqn. (1) shows that decreasing the back-gate voltage of the N-type fin results in the increase of $V_{th}$ of the front-gate-controlled N-type FET and therefore an exponential decrease of the leakage current.

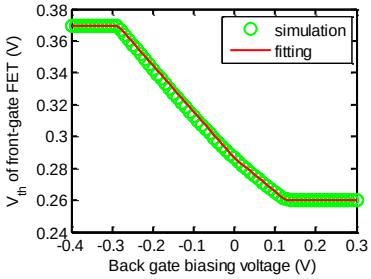


**Figure 1. $V_{th}$ of front-gate-controlled N-type FET v.s. back-gate voltage.**

Figure 1 shows the relationship between the threshold voltage of the front-gate-controlled FET and back-gate voltage from the Hspice simulation. Please note that the threshold voltage will not further decrease (or increase) when we increase back-gate voltage larger than a special value $V_{BN,max}$ or smaller than a special voltage level $V_{BN,min}$.

Authors in [7][8][9] proposed and applied different implementation modes of FinFET logic gates to exploit the unique feature of independent gate control. For the N-type or P-type fin, there are two different connection modes: (i) the double gate (DG) mode, where the front gate and the back gate of the fin are tied together to the input signal, and (ii) the independent gate (IG) mode, where one of the gate is driven by the input signal and the other is connected to a biasing voltage or to the ground. These different modes achieve a trade-off between power consumption and rise/fall delay. We illustrate in Figure 2 two examples of implementations of an inverter with approximately the same rise and fall delays. In Figure 2 (a), we use the double gate mode for both the N-type and P-type fins. In Figure 2 (b), we use the independent gate mode for the N-type fin and double gate mode for the P-type fin. We may also use the independent gate mode for the P-type fin, which is however not considered due to space limitation.

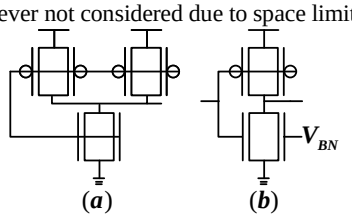


**Figure 2. Different FinFET inverters in different modes.**

### B. Driving Currents for FinFET Devices in the Near/Sub-Threshold Regime

The driving current is a critical parameter in FinFET modeling. In the subthreshold regime, the driving current $I_{FN}$ for the front-gate-controlled FET in an N-type fin follows an exponential relationship with the gate drive voltage $V_{FN}$ and the drain-to-source voltage $V_{ds}$. The equation is given by:

$$I_{FN} = I_0\frac{W}{L}\cdot e^{\frac{V_{FN}+\lambda V_{ds}-V_{th}(V_{BN})}{n\cdot v_T}}\left(1-e^{\frac{-V_{ds}}{v_T}}\right) \qquad (2)$$

where $I_0$ is a technology-dependent parameter, $\lambda$ is the drain voltage dependence coefficient (similar to but much smaller than the DIBL coefficient for bulk CMOS devices), $n$ is the subthreshold slope factor, and $v_T$ is the thermal voltage $\frac{kT}{q}$. Its threshold voltage $V_{th}$ is affected by the voltage $V_{BN}$ applied on the back gate of the same fin.

In order to consider the near-threshold regime as well, we extend the method of [17] for FinFETs to provide a unified transregional

model covering both subthreshold and near-threshold regimes. In this transregional model, the drain current $I_{FN}$ is given as:

$$I_{FN} = I_0 \frac{W}{L} \cdot e^{\frac{(V_{FN}+\lambda V_{ds}-V_{th}(V_{BN}))-a\cdot(V_{FN}+\lambda V_{ds}-V_{th}(V_{BN}))^2}{n\cdot v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right) \quad (3)$$

where $a$ is an empirical fitting parameter. We can extract the values of parameters $I_0$, $a$, and $n$ from HSpice simulations. The transregional model provides an accurate FinFET modeling in both subthreshold and near-threshold regimes when $V_{FN}$ (or $V_{BN}$) and $V_{ds}$ are equal. Based on our experiments, the average and maximal errors of the proposed transregional model are 4.27% and 8.83%, respectively, compared with HSpice simulations.

## III. Conventional Current Source-Based Modeling

The idea of current source-based modeling of logic cells was introduced about a decade ago with the goal of more accurately capturing the dependency of logic cell's timing behaviors on its input and output voltages. The CSM method builds an equivalent circuit model for each logic gate using independent current sources and several equivalent capacitors. An example of CSM for an inverter is presented in Figure 3.

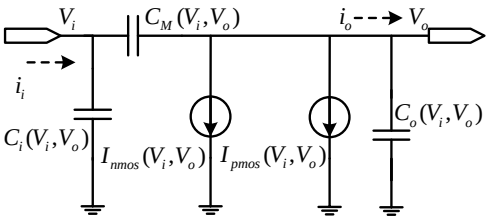


**Figure 3. Equivalent CSM for a CMOS inverter [14].**

In general, the CSM-based timing analysis is comprised of two phases: the characterization phase and the evaluation phase. In the characterization phase, an equivalent circuit model for each logic cell in the standard cell library is proposed and accurate circuit simulators (e.g., SPICE) are used to obtain the component values in the equivalent circuit model at different input and output voltages. In Figure 3, $V_i$ is the input voltage level and $V_o$ is the output voltage level of the inverter. Each component in Figure 3 is expressed as a function of $V_i$ and $V_o$. $C_i(V_i,V_o)$ and $C_o(V_i,V_o)$ denote the equivalent capacitances at the input and output nodes of the inverter, respectively, and $C_M(V_i,V_o)$ denotes the Miller capacitance. $I_o(V_i,V_o)$ denotes the driving current, which is the sum of $I_{nmos}(V_i,V_o)$ and $I_{pmos}(V_i,V_o)$. Multiple 2D LUTs are generated to store the above component values at different $V_i$ and $V_o$ levels, as shown in Figure 4.

In the evaluation phase, we calculate the output waveform of a logic cell using pre-characterized driving currents and equivalent capacitances, as well as sample values of the input voltage. The accuracy of the CSM method depends on both the LUT precision, i.e., *N* and *M* values in Figure 4, and the sampling precision, i.e., the number of sampling points in a certain time period, of the input waveform.

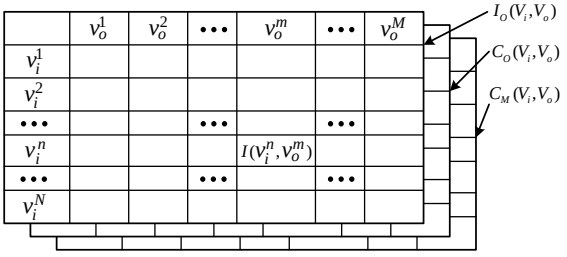


**Figure 4. Conventional 2D look-up tables for the CSM [14].**

CSMs for multiple-input logic cells such as NAND gates and NOR gates are more complex due to the existence of internal nodes, and will result in 3-D or 4-D LUTs. In order to reduce the storage overhead, several previous papers have focused on reducing the dimension of LUTs using approximation methods [24].

Both the driving current and parasitic capacitances can be significantly affected by process variations. Thus it is essential to account for the effects of variations of physical parameters in the CSM equivalent circuit model. A mathematical method is presented in [14] whereby the sensitivities of cell model elements are characterized with respect to the sources of variations. The nominal values of the LUTs are generated and a first-order (FO) correction is utilized to relate any component value in the logic cell with respect to the physical variation parameters. This process-variation induced CSM can be used to perform a statistical delay analysis for logic cells [14] or act as a fast Monte Carlo simulator.

## IV. Current Source Model for FinFET Devices

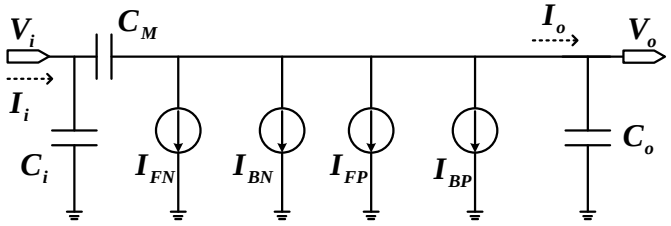


**Figure 5. Equivalent CSM for a FinFET inverter.**

To extend the CSM-based method to FinFET devices operating in near/sub-threshold voltage regimes, we should develop a model that can not only appropriately capture the variations of the component values in the equivalent circuit model due to the variations of process parameters, but also account for the effect that the threshold voltage of the front-gate-controlled FET is affected by the back-gate voltage, and vice versa. In this work, two major sources of process variations are considered in a FinFET transistor: *Line-Edge Roughness* (LER), which causes variations of the effective channel length, denoted by $\Delta L$, and *Gate Work-Function Variation* (WFV), which causes variations of the intrinsic threshold voltage, denoted by $\Delta V_{th0}$ [19]. Considering these effects, the CSM method utilizes an equivalent circuit model for the FinFET inverter as shown in Figure 5. Figure 5 is a general model in that it can represent the two implementations of FinFET inverters shown in Figure 2 (although the parameters may be different.) For the FinFET inverter shown in Figure 2 (a), we have $V_{FN} = V_{BN} = V_i$, whereas $V_{FN} = V_i$ and $V_{BN}$ is an additional biasing voltage for the FinFET inverter shown in Figure 2 (b). Given the values $V_{FN}$ ($V_{FP}$), $V_{BN}$ ($V_{BP}$), $V_{out}$, $\Delta L$ and $\Delta V_{th0}$ for both N-type and P-type FETs, we need to determine all the driving current and equivalent capacitance values shown in Figure 5.

One may extend the standard CSM LUTs to high dimensions to achieve this goal, e.g., storing different driving current values at various process parameter values and voltage levels. However, this simple treatment will result in an unacceptable memory space requirement. An alternative solution will be storing the LUTs when $\Delta V_{th0} = 0$ and $\Delta L = 0$, and apply polynomial corrections for process variations. However, this method turns out to be both inaccurate and cost-ineffective due to the following two reasons: (i) For FinFET devices operating in the sub/near-threshold regime, the relationship between the driving current and the gate voltages becomes exponential. (ii) The applied back-gate voltage exerts an influence on the threshold voltage of the front gate, and vice versa, which also significantly affects the timing behavior of the gate because the driving current is exponentially dependent on the threshold voltage. Hence, the polynomial correction method is not sufficient to capture the effects of the back-gate (and

front-gate) voltage and process variations for FinFET devices operating in sub/near-threshold regime.

In order to achieve higher modeling accuracy while maintaining time/space efficiency, we propose an efficient way to construct a semi-analytical CSM for the FinFET logic cells in this section based on the physical relations of the current, gate voltages and process parameters. Notice that we only use 2D LUTs in the proposed method to reduce the storage space requirement. In Section IV.A, we capture the change of threshold voltage of the front(back)-gate-controlled FET as a function of the back(front)-gate voltage and process variations. In Section IV.B, we analyze the modeling of the driving current of a fin with respect to the threshold voltages of both the front-gate-controlled and back-gate-controlled FETs and the variation of the effective channel length. Section IV.C focuses on the modeling of parasitic capacitances, and finally, the CSM LUT construction process is summarized in Section IV.D.

Please note that although we mainly describe FinFET inverters in this paper, the semi-analytical modeling framework can also be generated to the other types of FinFET gates, such as NAND and NOR gates. The generalization process will be similar to [24], and is not discussed in detail in this paper due to space limitation.

### A. The Impact on the Threshold Voltage

We use a piecewise linear function to represent the impact of the back-gate voltage $V_{BN}$ on the change of the threshold voltage $\Delta V_{th}(V_{BN})$:

$$\Delta V_{th}(V_{BN}) = \begin{cases} \Delta V_{th,max}, & V_{BN} < V_{BN,min} \\ k_1 V_{BN}, & V_{BN,min} \le V_{BN} < 0 \\ k_2 V_{BN}, & 0 \le V_{BN} < V_{BN,max} \\ \Delta V_{th,min}, & V_{BN} \ge V_{BN,max} \end{cases} \quad (4)$$

There are four fitting parameters in the above equation: $k_1$, $k_2$, $V_{BN,min}$, $V_{BN,max}$. $k_1$ and $k_2$ represent the $\frac{dV_{th}}{dV_{BN}}$ values in Eqn. (1) when $V_{BN} < 0$ and $V_{BN} > 0$, respectively, and are both less than 0. Notice that in general $k_1$ and $k_2$ are not equal, which means that the capacitances $C_{si}$, $C_{oxf}$, and $C_{oxb}$ are not exactly the same when $V_{BN} < 0$ (i.e., reverse back-gate biasing) and $V_{BN} > 0$ (i.e., forward back-gate biasing.) Similarly, $\Delta V_{th}(V_{FN})$ is the threshold voltage change of the back-gate-controlled FET as a function of the front-gate voltage $V_{FN}$, which also satisfies Eqn. (4). In our experiment, we have the fitting results ($k_1$, $k_2$, $V_{BN,min}$, $V_{BN,max}$) = (-0.2897, -0.2098, -0.29V, 0.12V).

Gate Work-Function Variation (WFV) is another important type of variation source which causes the variability of the threshold voltage. We denote the threshold voltage variation caused by WFV as $\Delta V_{th0}$. Experimental results show that the fitting parameters in Eqn. (4) are independent of $\Delta V_{th0}$.

In bulk CMOS, the threshold voltage $V_{th}$ also depends on the variation of channel length due to the *drain-induced barrier lowering* (DIBL) effect. This effect is more pronounced in short-channel devices in the state-of-the-art CMOS technology [20], and *Halo doping* is used to compensate the DIBL effect, which will result in an opposite *reverse short channel effect* [21]. One the other hand, FinFET devices has a significantly reduced DIBL effect due to the more effective channel control by the gate voltages, which is one of the primary advantages [22] of the FinFET technology. Based on our experimental result on the 32nm PTM, $\Delta L$ has almost no effect on the threshold voltage for FinFET devices.

In summary, the threshold voltage of the front-gate-controlled FET, considering both the back-gate voltage and process variations, is given by

$$V_{th,F} = V_{th0} + \Delta V_{th}(V_{BN}) + \Delta V_{th0} \quad (5)$$

Similarly, the threshold voltage of the back-gate-controlled FET is given by $V_{th,B} = V_{th0} + \Delta V_{th}(V_{FN}) + \Delta V_{th0}$. Please note that the $V_{th0}$ and $\Delta V_{th0}$ values are the same in both equations because both the front and back gates share the same fin. Experimental results show that the average and maximal fitting errors are 0.3% and 0.94%, respectively.

### B. Modeling of the Driving Current

In the standard CSM shown in Figure 3, the driving current at the output node is a combination of the NMOS current, $I_N(V_i, V_o)$, and the PMOS current, $I_P(V_i, V_o)$. Thus, we characterize $I_N(V_i, V_o)$ and $I_P(V_i, V_o)$ for all possible combinations of $V_i$ and $V_o$, which results in a set of 2-D lookup tables. For FinFET devices with the independent gate control and process variations, our goal is to use no larger than 2-D lookup tables to determine the driving current $I_N$ (and $I_P$) under the applied voltage levels, i.e., $V_{FN}$, $V_{BN}$ and $V_{ds}$, and specific process variation parameters, i.e., $\Delta L$ and $\Delta V_{th0}$. Considering that each fin is essentially a parallel connection of the front-gate-controlled FET and the back-gate-controlled FET, $I_N$ (or $I_P$) is the sum of the driving current of the front gate and that of the back gate:

$$I_N = I_{FN} + I_{BN} \quad (6)$$

Take the front gate of the N-type fin as an example. We fit $I_{FN}$ with respect to $\Delta L$ and $\Delta V_{th0}$ based on Eqn. (3) in the near/sub-threshold regime using the following form:

$$I_{FN}(V_{FN}, V_{BN}, V_{ds}, \Delta L, \Delta V_{th0}) = \frac{\mathbf{C}(V_{FN}, V_{ds})}{L} \cdot e^{\mathbf{A}(V_{FN}, V_{ds}) \cdot V_{th,F}^2 + \mathbf{B}(V_{FN}, V_{ds}) \cdot V_{th,F}} \quad (7)$$

where $\mathbf{A}(V_{FN}, V_{ds})$, $\mathbf{B}(V_{FN}, V_{ds})$, and $\mathbf{C}(V_{FN}, V_{ds})$ are fitting parameters. The dependencies of the driving current on $V_{FN}$ and $V_{ds}$ in Eqn. (3) are absorbed into these fitting parameters. The value $L = L_0 + \Delta L$ where $L_0$ is the nominal effective length. The value $V_{th,F}$ depends on $\Delta V_{th}(V_{BN})$ as well as the WFV parameter $\Delta V_{th0}$, as is shown in Eqn. (5). Notice that the front gate and the back gate have the symmetric structure. Hence, the same fitting parameters can be used to calculate the current of the back gate:

$$I_{BN}(V_{FN}, V_{BN}, V_{ds}, \Delta L, \Delta V_{th0}) = \frac{\mathbf{C}(V_{BN}, V_{ds})}{L} \cdot e^{\mathbf{A}(V_{BN}, V_{ds}) \cdot V_{th,B}^2 + \mathbf{B}(V_{BN}, V_{ds}) \cdot V_{th,B}} \quad (8)$$

The above method combines the non-linear analytical models and small-size CSM lookup tables, and simultaneously achieves high modeling accuracy and space/time efficiency. Compared with Eqn. (3), the lookup table-based model Eqns. (7) and (8) results in much higher accuracy (please see the experimental results) because some parameters in Eqn. (3), such as the subthreshold slope $n$, depend on $V_{FN}$ and $V_{ds}$ [25]. Moreover, the effect of $V_{BN}$ on $V_{th,F}$ (and $V_{FN}$ on $V_{th,B}$) and that of process variations are carefully accounted for without increasing the model complexity, since we are still using 2-D LUTs to store all the fitting parameters, like what is used in the standard CSM for bulk CMOS devices. Similarly, the proposed method can be applied to the P-type fin to determine the corresponding driving current $I_P$.

### C. Modeling of Parasitic Capacitances

In this section, we analyze the impact of process variations on the values of equivalent capacitance in the CSM equivalent circuit model as shown in Figure 5. This equivalent circuit model is comprised of three non-linear voltage-dependent capacitances. Among then, $C_i$ and $C_o$ model the parasitic effects at the input and output nodes of the logic cell, whereas the Miller capacitance $C_M$ models the Miller effect between these two nodes. Notice that for FinFET devices, these equivalent parasitic capacitances are contributed by the physical capacitances (e.g., $C_{gs}$, $C_{gd}$, $C_{db}$ and so on) in both the front-gate-controlled and back-gate-controlled FETs in both the N-type and P-type fins.

We know that the equivalent capacitance values will be very different for the FinFET inverter shown in Figure 2 (a) and that in Figure 2 (b) due to different connection modes. Hence, we need to consider these two modes separately in the parasitic capacitance modeling. Take the inverter shown in Figure 2 (b) as an example. Both the process variations as well as the biasing voltage level $V_{BN}$ will

affect the equivalent capacitance values. For example, the LER effect affects the capacitance values as these capacitances are functions of the dimension of the transistors. In addition, the bias voltage also exerts an effect on the parasitic capacitances. Therefore, we perform curve fitting to relate the equivalent capacitances to the process parameters as well as the bias voltage $V_{BN}$ for each $(V_i, V_o)$ pair. As the effects of process variations and bias voltage on parasitic capacitances are relatively small compared with those on the driving current, experimental results show that the linear curve fitting is able to capture the dependency of the equivalent capacitances on the above-mentioned parameters. The variations of process parameters originate from both N-type and P-type fins, and thus the equivalent capacitance $C_i$ is fitted as follow,

$$\begin{aligned} &C_i(V_i, V_o, \Delta L_P, \Delta L_N, \Delta V_{th0P}, \Delta V_{th0N}, V_{BN}) \\ &= \mathbf{C}_{i0}(V_i, V_o) + \boldsymbol{\alpha}_P(V_i, V_o) \cdot \Delta L_P + \boldsymbol{\alpha}_N(V_i, V_o) \cdot \Delta L_N \\ &+ \boldsymbol{\gamma}_P(V_i, V_o) \cdot \Delta V_{th0P} + \boldsymbol{\gamma}_N(V_i, V_o) \cdot \Delta V_{th0N} + \boldsymbol{\delta}_N(V_i, V_o) \cdot V_{BN} \end{aligned} \quad (9)$$

where $\mathbf{C}_{i0}$ is the LUT of the nominal input capacitance values in CSM, $\Delta L_P$ and $\Delta L_N$ are the variations of the channel length in the N-type fin and P-type fin, respectively. $\Delta V_{th0P}$ and $\Delta V_{th0N}$ are the WFV-induced threshold voltage variations in the N-type fin and P-type fin, respectively. Similar fittings are also performed for $C_o$ and $C_M$.

The same fitting method can be used for the FinFET inverter shown in Figure 2 (a), except that no separate bias voltage exists in this inverter. Hence, we do not need the parameter $\boldsymbol{\delta}_N(V_i, V_o)$ in Eqn. (9).

### D. CSM LUT Construction

After studying the modeling of driving current and the parasitic capacitances, the CSM LUT construction process can be concluded as follows: in the characterization phase, we perform characterization as well as curve fitting as mentioned earlier and record the coefficient into the LUTs with index of interested voltage levels. In the evaluation phase, we use the coefficient LUTs to construct the customized CSM LUTs including $I_o$, $C_M$, $C_i$ and $C_o$ under every voltage pair $(V_i, V_o)$, under different corners of process variation parameters and bias voltage levels, e.g., $\Delta L$, $\Delta V_{th0}$ and $V_{BN}$(or $V_{FN}$). The constructed CSM LUTs can be used to calculate the exact output waveform given the waveform of the input voltage.

The proposed semi-analytical CSM method enables accurate current-based timing analysis at various process corners and bias voltage levels without increasing the dimension (and thus the time/space complexity) of the conventional LUTs. In practice, although it is generally hard to know the detailed amounts of the variation (as the variations of the process parameters are random and usually normally described), the statistical method can be utilized to obtain the accurate joint distributions of the process parameters and reflect their variations statistically into the flow of constructing the standard CSM LUTs. With these distributions, we can perform the current-based statistical timing calculation using the proposed semi-analytical CSM method to study the distribution of the parameters of the output waveform. e.g., the delay and the transition time.

## V. Experimantal Results

In this section, we evaluate the accuracy of the proposed semi-analytical CSM for FinFET devices in calculating the output waveform and delay. We adopt 32nm Predictive Technology Model for FinFET devices, in which the typical threshold voltages of the transistors are around ±0.3V. We set the supply voltage to 0.3V so that the circuits are operated in the near/sub-threshold regime. To ensure that voltage characterization covers the range of the noise, we sweep the input and output voltage from -100 mV to +400 mV with the interval of 5 mV. We consider 10% variation on the process parameters $\Delta L$ and $\Delta V_{th0}$, and apply different bias voltage levels from -0.4V to 0.3V. The characterization is based on HSPICE, and the entire process for FinFET modeling and output waveform calculating takes less than an hour on a Debian 7 machine with 16 Intel E7-8837 2.66 GHz CPUs and 64 GB memory.

We compare our work with the CSM with first order correction like [14] in handing bias voltage and process variations. The proposed method and baseline method are compared to the golden results generated using the HSPICE considering input noises. The fitting result of the impact of the back-gate voltage $V_{BN}$ on the change of the threshold voltage $\Delta V_{th}(V_{BN})$ is already shown in the previous sections. In this section, we first verify the accuracy of the proposed semi-analytical CSM method in capturing the driving currents at different corners of process variations. After that, we demonstrate the accuracy of proposed CSM in calculating the real output waveforms under a noise input.

### A. Modeling of the FinFET driving current

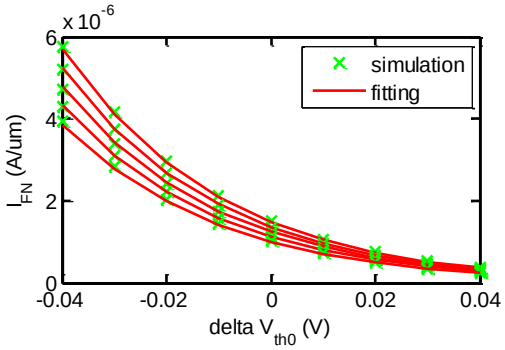


**Figure 6. Curve fitting of N-type FET driving current under different corners of process variation.**

Due to space limitation, we only show the fitting result of the driving current of N-type FET in Figure 6 under different corners of process variation parameters $\Delta L$ and $\Delta V_{th0}$ at the voltage pair $(V_{FN}, V_{ds}) = (0.1V, 0.2V)$. Our proposed method achieves very good fitting quality with an average error of 0.81%. The fittings of the driving currents are performed for every point $(V_{FN}, V_{ds})$.

### B. Output waveform under noisy input

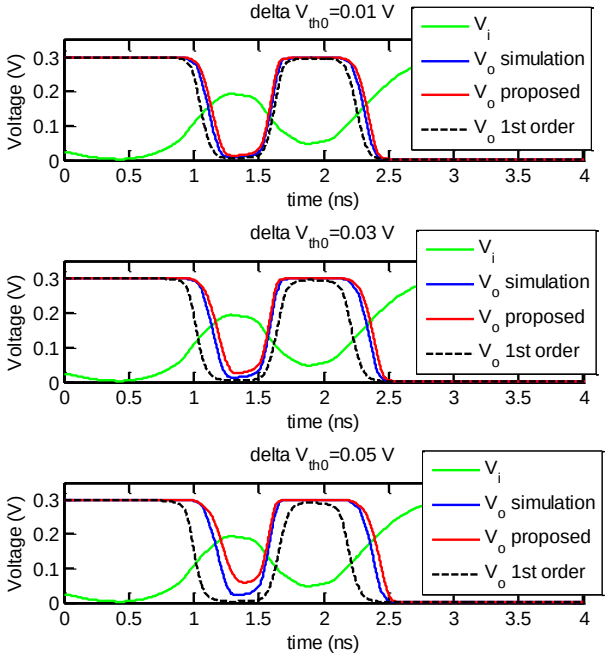


**Figure 7. Output waveforms for different CSM variation handing techniques under a noise input at different threshold voltage variation levels.**

We generate the customized CSM LUTs to calculate the output waveforms based on the pre-characterized LUTs with respect to different process variation parameters. We show the DG-mode inverter as an example and calculate output waveforms and compare them with the waveforms obtained using HSPICE simulation. Figure 7 shows three cases of $\Delta V_{th0}$ variation levels: 0.01V, 0.03V, and 0.05V, while $\Delta L$ is set to 1nm. The proposed CSM method consistently outperforms the first-order method. It reproduces the output waveform with a very high accuracy and achieves an average delay error reduction of more than 60% compared with the baseline first-order method. Among these two methods, the detailed comparison of the 50%-50% delay calculation errors at each transition point for different output waveforms is shown in Table 1. The high accuracy and low space requirement ensure the capability of performing statistical timing calculation and analysis based on the proposed CSM method, with the combination of some statistical tools.

**Table 1. The delay error comparison for different output waveforms.**

| $\Delta L$ = 1nm, $\Delta V_{th0}$ = 0.01V | | | |
|---|---|---|---|
| | Point 1 | Point 2 | Point 3 |
| Proposed method | 2.33% | 0.63% | 1.03% |
| First-order method | 5.21% | 1.63% | 2.42% |
| $\Delta L$ = 1nm, $\Delta V_{th0}$ = 0.03V | | | |
| | Point 1 | Point 2 | Point 3 |
| Proposed method | 3.31% | 0.76% | 1.37% |
| First-order method | 10.82% | 3.66% | 5.38% |
| $\Delta L$ = 1nm, $\Delta V_{th0}$ = 0.05V | | | |
| | Point 1 | Point 2 | Point 3 |
| Proposed method | 4.57% | 0.38% | 1.94% |
| First-order method | 15.03% | 5.34% | 7.43% |

## VI. CONCLUSION

In this paper, we present a semi-analynical current source modeling (CSM) method for FinFET devices operating in the near/sub-threshold voltage regime, accounting for the independent gate control and process variations. The driving currents and parasitic capacitances are analyzed under different bias voltages and process varations in the near/sub-threshold regime. A curve fitting step is performed to relate the driving currents and parasitic capacitances to the bias voltage levels as well as the sources of process variations, and fitting parameters are stored in low-dimentional look-up tables (LUTs). In circuit timing simulation, we derive the driving current and equivalent capacitances under the specific back-gate(or front-gate) bias voltage and process variation situation in practice. Experimental results demostrate the effectiveness of the proposed framework in both modeling accuracy and efficiency.

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